

MODEL NAME : *FDV40*  
PCB NO : *LA-J541P*  
BOM P/N : *431AKI31LXX*

**Dell/Compal Confidential**  
**Schematic Document**  
**(Spyglass MLK Comet Lake U)**

**BOM Structure**

- @ : Nopop Component
- RF@ : RF Component
- @RF@ : RF Nopop Component
- EMI@ : EMI Component
- @EMI@ : EMI Nopop Component
- 5107ES@ : Option for MEC5107 ES
- 5107NES@ : Option for MEC5107 NES
- ST@ : ST TPM
- 750@ : Nuvoton TPM
- NRTD3@ : non RTD3 support
- RTD3@ : RTD3 support
- NDS3@ : non Deep sleep support
- DS3@ : Deep sleep support
- XDP@ : XDP Component
- DB@ : Debug Component
- BreakDown@ : Breakdown Component
- VPRO@ : VPRO CPU
- NVPRO@ : NVPRO CPU
- RTK@ : Codec Component
- WOA@ : Codec Component

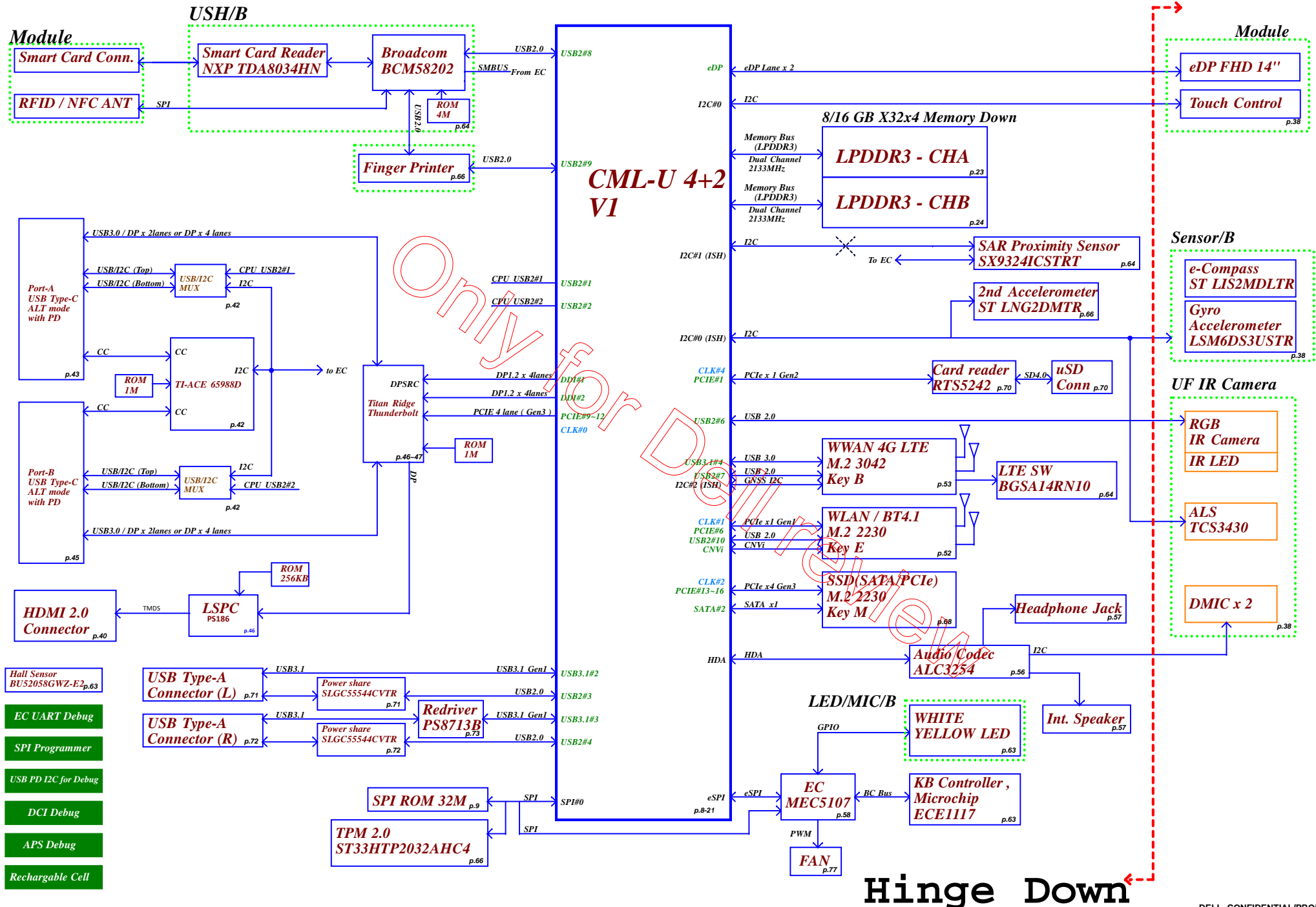
2020-03-04

Rev:1.0(A00)

- ESD@ : ESD Component
- @ESD@ : ESD Nopop Component
- OS@ : S5 LID Open
- RC@ : Replace S5 LID open

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Date: Wednesday, March 04, 2020		Sheet 1 of 100		P001 - Cover	
				LA-J541P	

# Hinge up

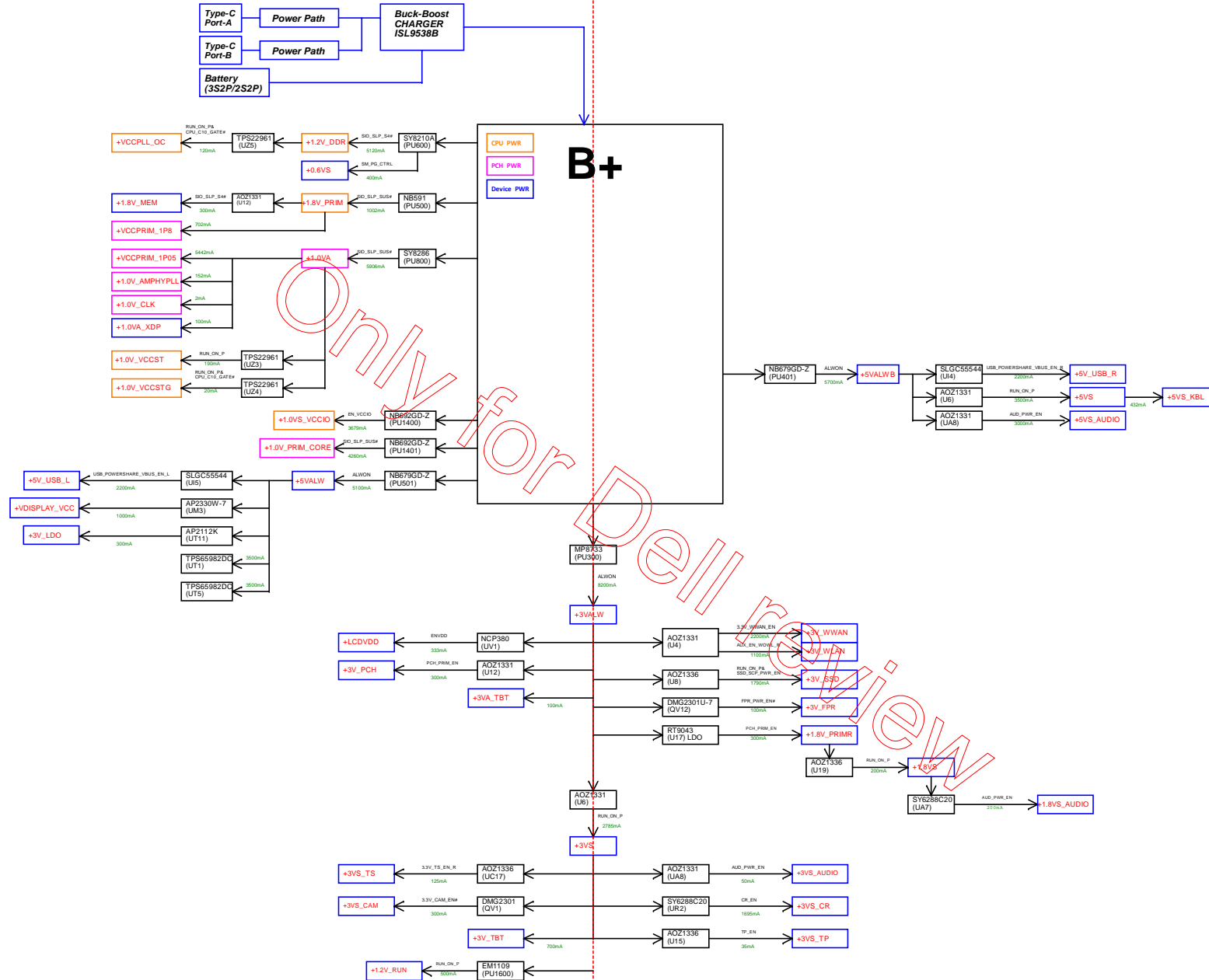


## Hinge Down

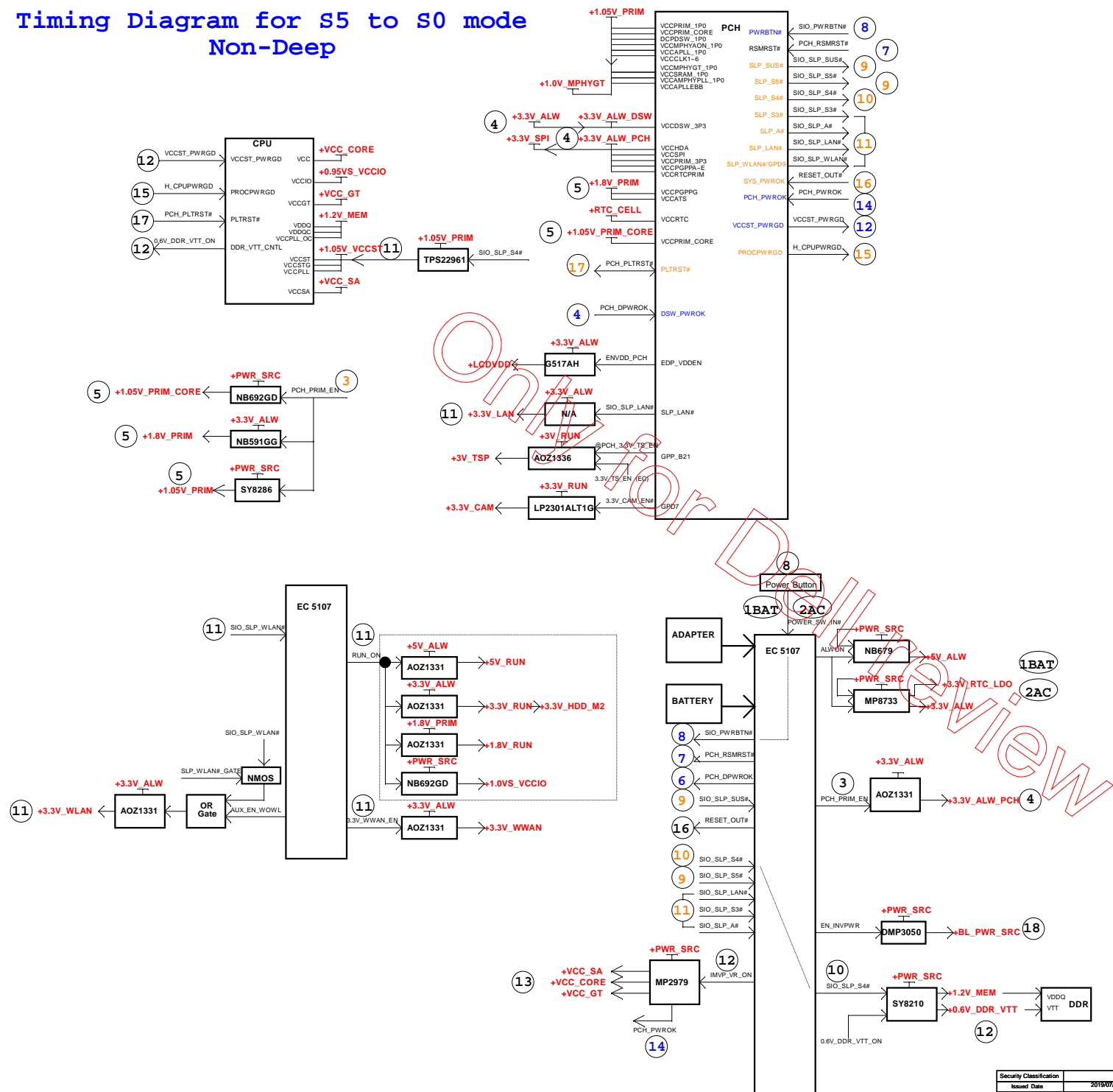


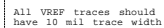
Left Side

Right Side

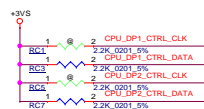


### Timing Diagram for S5 to S0 mode Non-Deep





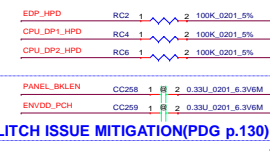
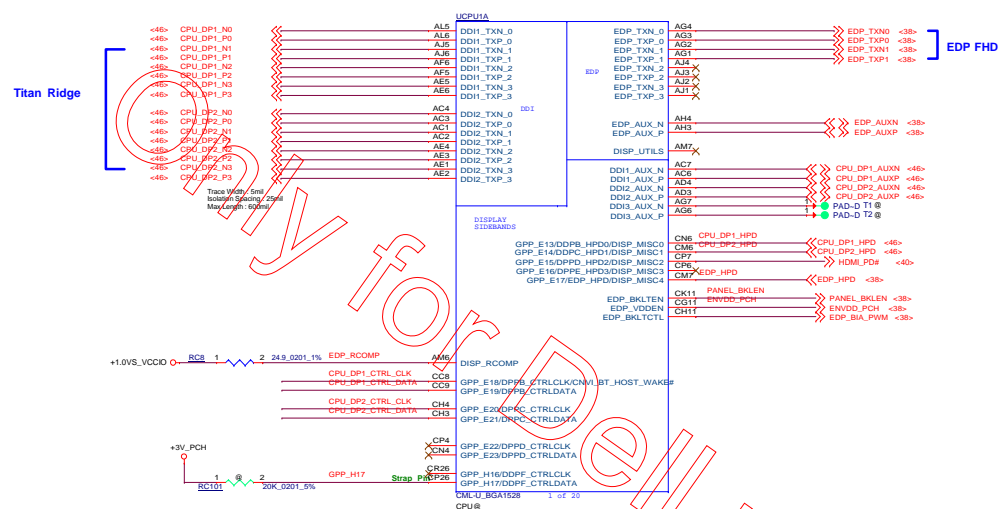
COMPENSATION PU FOR eDP  
CAD Note:  
Trace width=5 mils  
Isolation Spacing=25mil,  
Max length=100 mils.



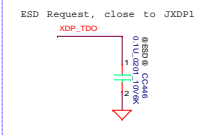
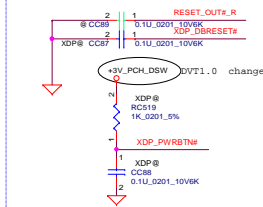
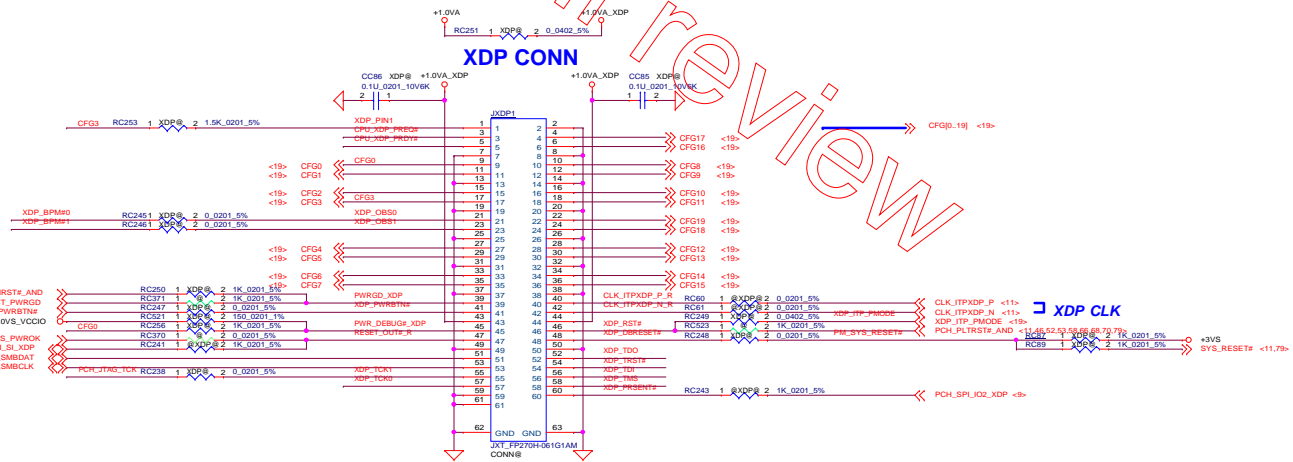
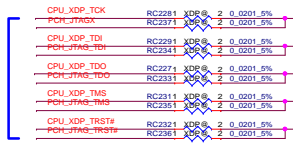
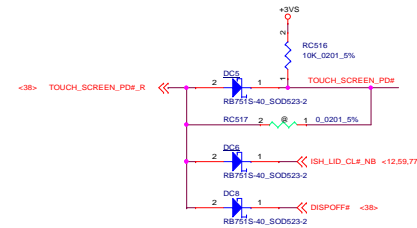
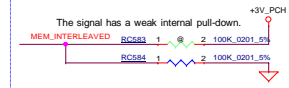
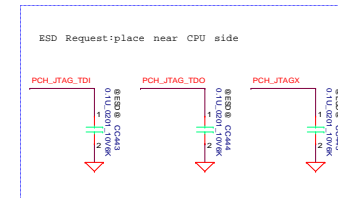
**GPP\_E19 (WEAK INTERNAL PD)**  
 0 = Port B is not detected. (Default)  
 1 = Port B is detected.

**GPP\_E21 (WEAK INTERNAL PD)**  
 0 = Port C is not detected. (Default)  
 1 = Port C is detected.

**GPP\_E23 (WEAK INTERNAL PD)**  
 0 = Port D is not detected. (Default)  
 1 = Port D is detected.

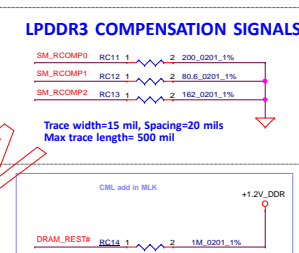


PCH GLITCH ISSUE MITIGATION(PDG p.130)





## UCPU1C



SM\_RCOMP0 RC11 1 2 200\_0201\_1%

SM\_RCOMP1 RC12 1 2 80.6\_0201\_1%

SM\_RCOMP2 RC13 1 2 162\_0201\_1%

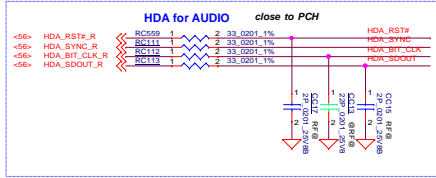
Trace width=15 mil, Spacing=20 mils  
Max trace length= 500 mil



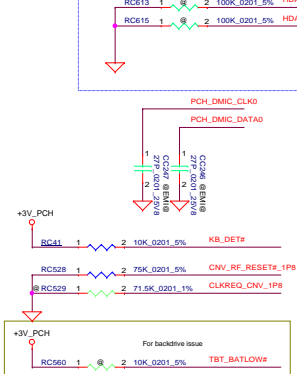




Capacitor to only be used for HDA\_SDO, HDA\_RST#, and HDA\_SDI for EMI purposes and should be as close as possible to the PCH.  
For HDA\_SDO and HDA\_RST# the cap should be after the series resistor closest to the PCH.



**PCH GLITCH ISSUE MITIGATION(PDG p.130)**



**TOP SWAP OVERRIDE**

GPP\_B14 / SPKR (WEAK INTERNAL PD)

0 = Disable Top Swap mode. (Default)

1 = Enable Top Swap mode.

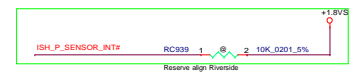
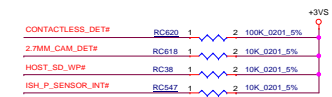
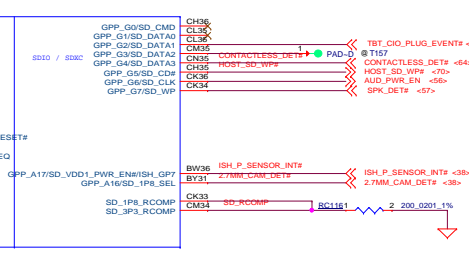
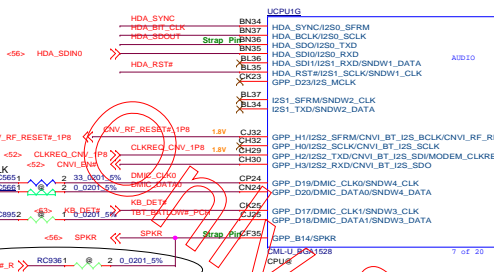
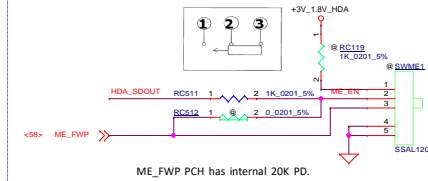


**Flash Descriptor Security Override**

HDA\_SDO / I2S0\_TXD (WEAK INTERNAL PD)

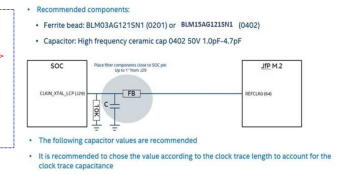
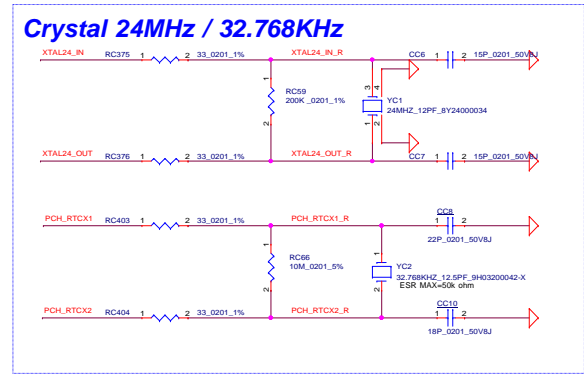
Disable ME Protect (ME can be updated) ----> Pin1 & Pin2 short

Enable ME Protect (ME cannot be updated)-->Pin3 & Pin2 short(Default position)

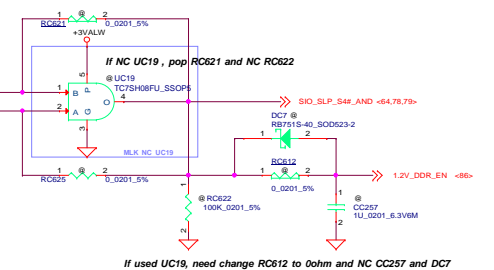
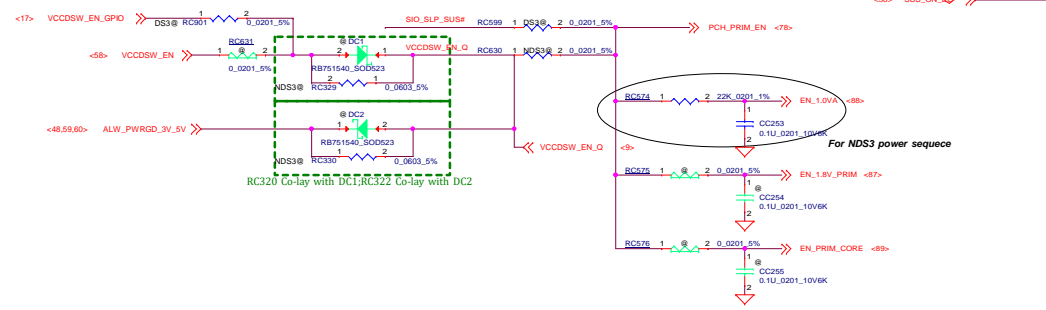
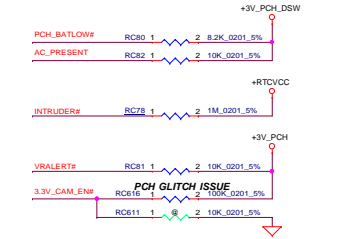
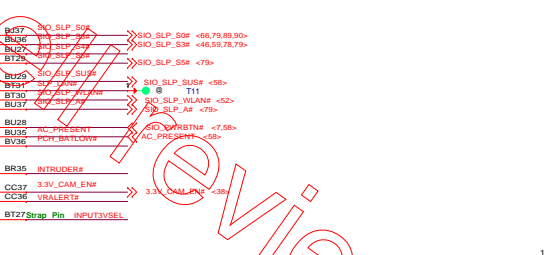
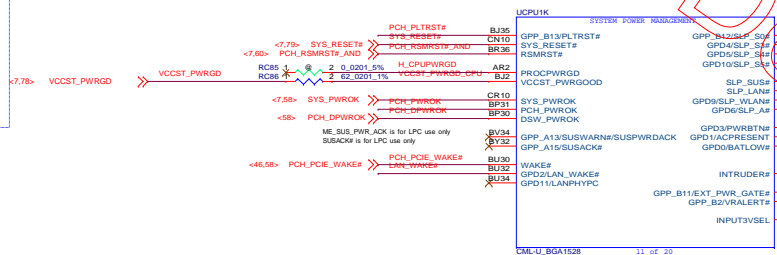
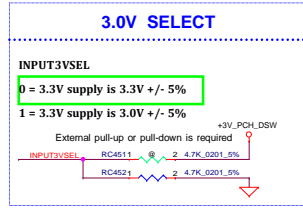


Reserve for EC control top swap

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Clock route length = L	Recommended capacitor values
$L < 5''$	4.7pF
$5'' < L < 9''$	2.2pF to 3.3pF
$9'' < L < 10''$	1.0pF to 2.2pF



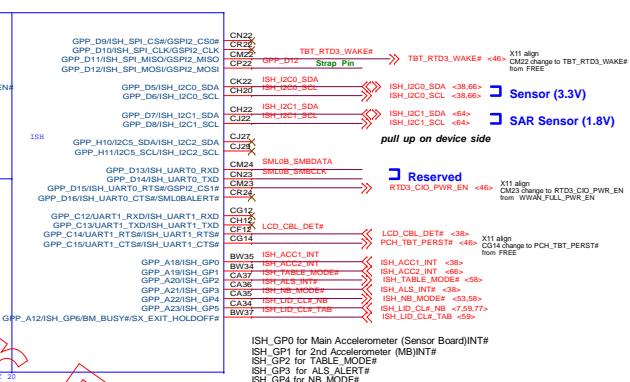
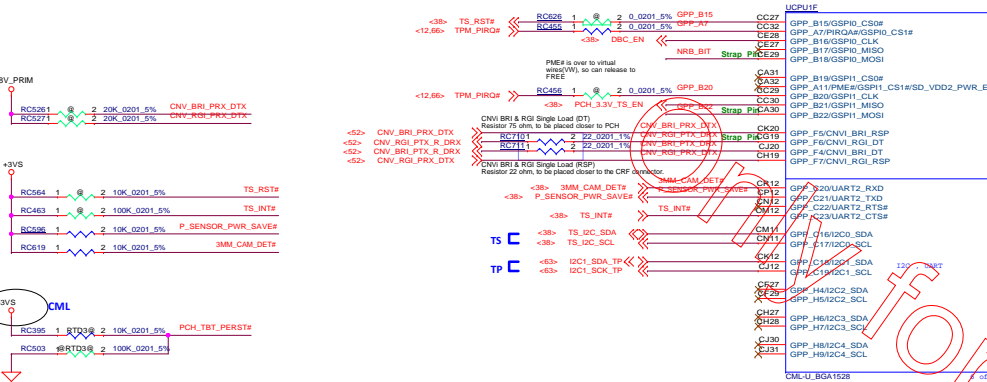
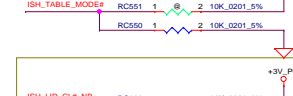
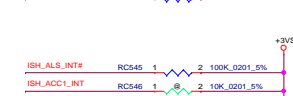
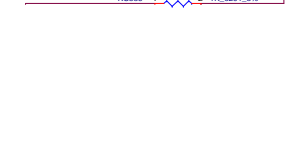
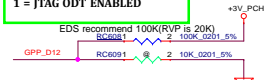
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Issued Date		2019/07/23		Deciphered Date		2022/12/31		Title <b>Compal Electronics, Inc.</b> <b>P011 - CML-U(6/14)CLK,PM,RTC</b>	
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						Date:		Wednesday, March 04, 2020	
						Sheet		11 of 100	

**JTAG ODT DISABLE**

**GPP\_D12 (WEAK INTERNAL PU)**

0 = JTAGE ODT DISABLED

1 = JTAG ODT ENABLED



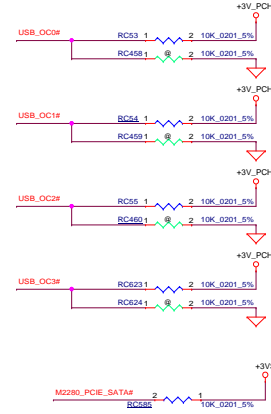
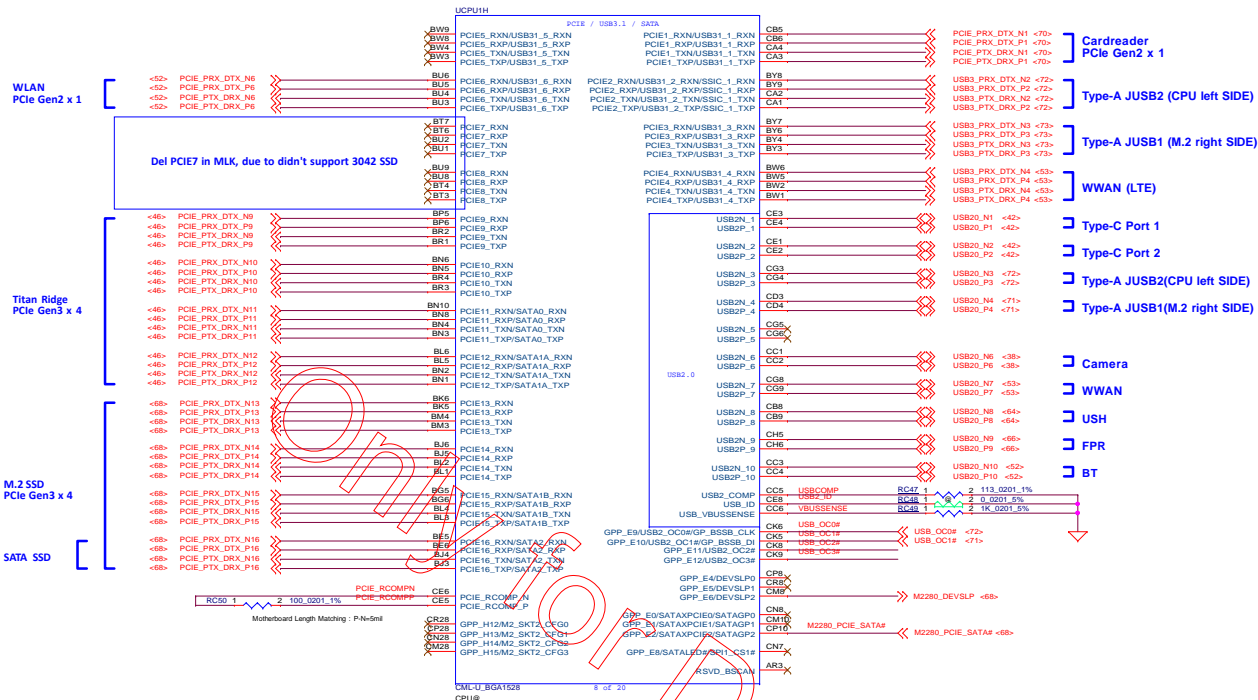
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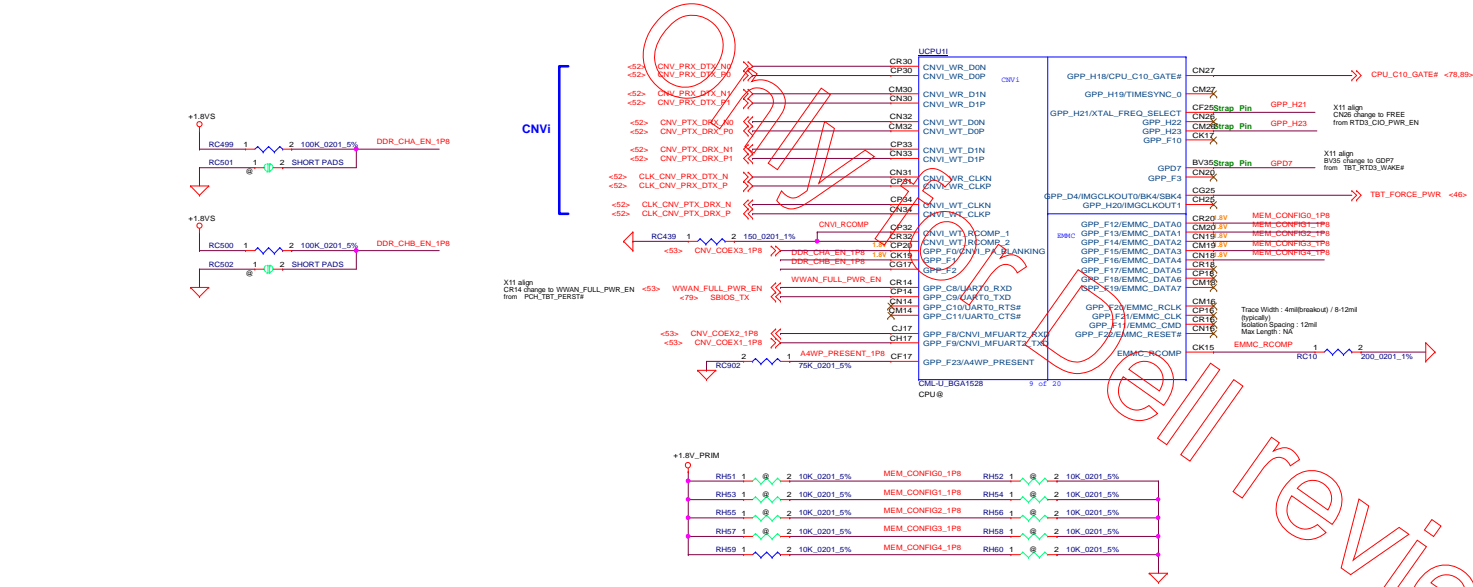
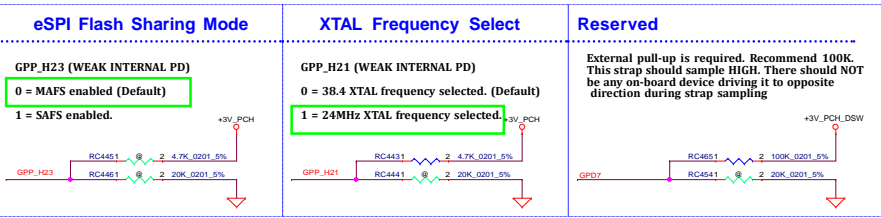
ISH_GP0 for Main Accelerometer (Sensor Board)INT#
ISH_GP1 for 2nd Accelerometer (MB)INT#
ISH_GP2 for TABLE_MODE#
ISH_GP3 for ALS_ALERT#
ISH_GP4 for NB_MODE#
ISH_GP5 for NB_LID#
ISH_GP6 for TAB_LID#
ISH_GP7 for Proximity sensor(Camera)INT#

```

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Title		
<b>P012 - CML-U(7/14)I2C,UART,ISH</b>		
Size	Document Number	Rev
	<b>LA-J541P</b>	<b>1.0(A00)</b>
Date:	Wednesday, March 04, 2020	Sheet 12 of 100





DDR Memory Configuratio Type Strap pin

GPIO Pin	Pin Name		Micron 8Gb (4Gb)	Micron 16Gb (8Gb)	Micron 32Gb (16Gb)	Rynix 8Gb (4Gb)	Rynix 16Gb (8Gb)	Rynix 32Gb (16Gb)	Samsung 8Gb (4Gb)	Samsung 16Gb (8Gb)	Samsung 32Gb (16Gb)	Nanya 16Gb (8Gb)	Nanya 32Gb (16Gb)
GPP_F12	MEM_CONFIG0	2133 Mbps	0	1	0	1	0	1	0	1	0	1	0
GPP_F13	MEM_CONFIG1		1	1	0	0	1	1	0	0	1	0	1
GPP_F14	MEM_CONFIG2		0	0	1	1	1	1	0	0	0	1	1
GPP_F15	MEM_CONFIG3		0	0	0	0	0	0	1	1	1	1	1
GPP_F16	MEM_CONFIG4		1	1	1	1	1	1	1	1	1	1	1

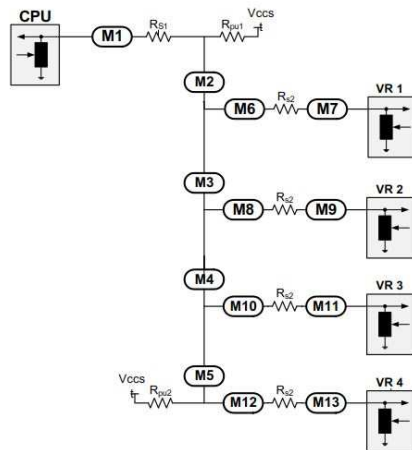
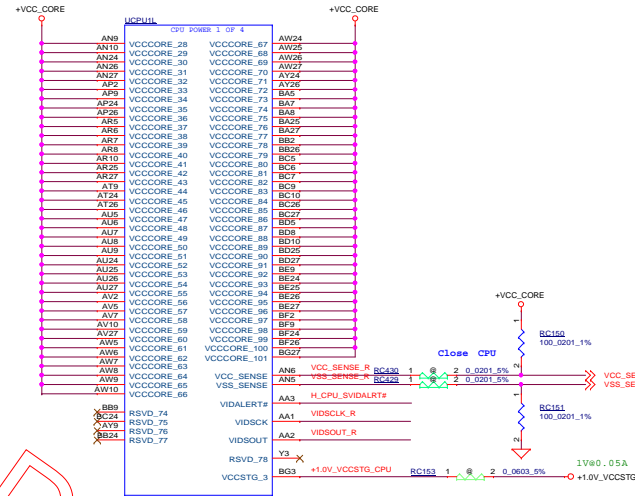
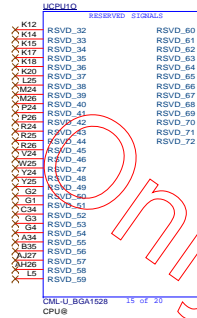
Pin Number	CTL Data	WHL U42 Q6/Production	CML U42/WHL U42 ES01.1
AV28	29M	RSVD	RSVD
V25	VCCOPD_SENSE	RSVD	RSVD
V25	VCCOPD_SENSE	RSVD	RSVD
AA34	VCCOPD	RSVD	RSVD
AA36	VCCOPD	RSVD	RSVD
AA35	VCCOPD	RSVD	RSVD
AA34	VCCOPD	RSVD	RSVD
AA35	VCCOPD	RSVD	RSVD
AA36	VCCOPD	RSVD	RSVD
AA37	VCCOPD	RSVD	RSVD
AA38	VCCOPD	RSVD	RSVD
AA39	VCCOPD	RSVD	RSVD
AA40	VCCOPD	RSVD	RSVD
AA41	VCCOPD	RSVD	RSVD
AA42	VCCOPD	RSVD	RSVD
AA43	VCCOPD	RSVD	RSVD
AA44	VCCOPD	RSVD	RSVD
AA45	VCCOPD	RSVD	RSVD
AA46	VCCOPD	RSVD	RSVD
AA47	VCCOPD	RSVD	RSVD
AA48	VCCOPD	RSVD	RSVD
AA49	VCCOPD	RSVD	RSVD
AA50	VCCOPD	RSVD	RSVD
AA51	VCCOPD	RSVD	RSVD
AA52	VCCOPD	RSVD	RSVD
AA53	VCCOPD	RSVD	RSVD
AA54	VCCOPD	RSVD	RSVD
AA55	VCCOPD	RSVD	RSVD
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AA66	VCCOPD	RSVD	RSVD
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AA68	VCCOPD	RSVD	RSVD
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AA91	VCCOPD	RSVD	RSVD
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AA97	VCCOPD	RSVD	RSVD
AA98	VCCOPD	RSVD	RSVD
AA99	VCCOPD	RSVD	RSVD
AA100	VCCOPD	RSVD	RSVD

PSC(Primary side cap) : Place as close to the package as possible  
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:  
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

+VCC\_CORE: 0.55~1.5V, 29A  
+VCC\_EDRAM: 1V, 2.5A

+V1.8S\_EDRAM: 1.8V, 50mA - REMOVE  
+VCC\_EOPIO: 0.8~1V, 2A - REMOVE



VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω

VCCOPC,VCCOPC\_1P8,VCCEOPIO for SKYLAKE-U 2+3e  
(w/ on package cache)

SVID ALERT

SVID DATA

SVID CLK

CAD Note: Place the PU resistors close to CPU  
RC154 close to CPU 1000 - 1500mils

CAD Note: Place the PU resistors close to CPU  
RC156 close to CPU 1000 - 1500mils

CAD Note: Place the PU resistors close to CPU  
RC158 close to CPU 1000 - 1500mils

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Security Classification	Compal Secret Data
Issued Date	Deciphered Date
2019/07/23	2022/12/31

Title	Part Number
P015 - CML-U(10/14)CORE Power	LA-J541P
Rev	1.0/400

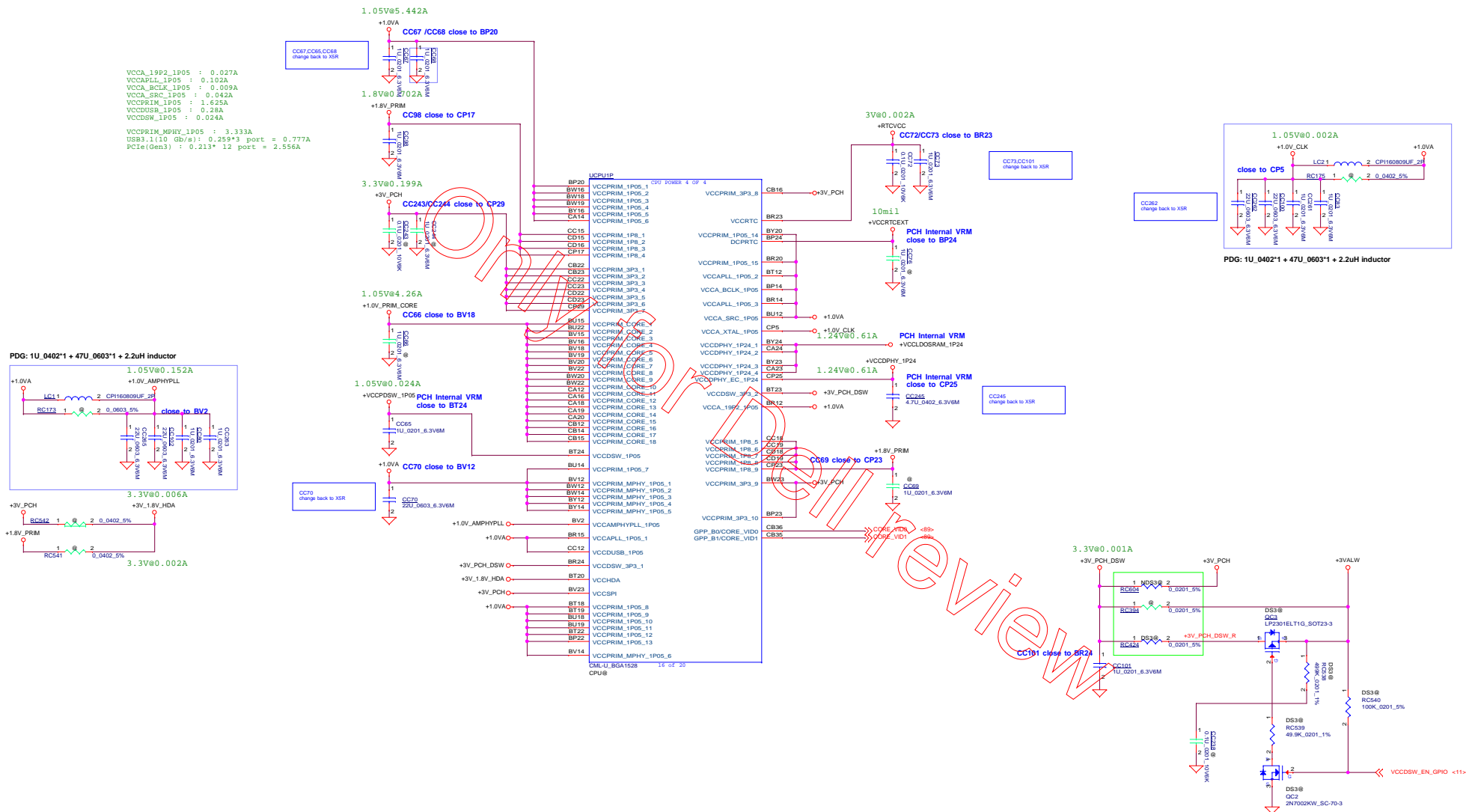
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Date: Wednesday, March 04, 2020 Sheet 15 of 100



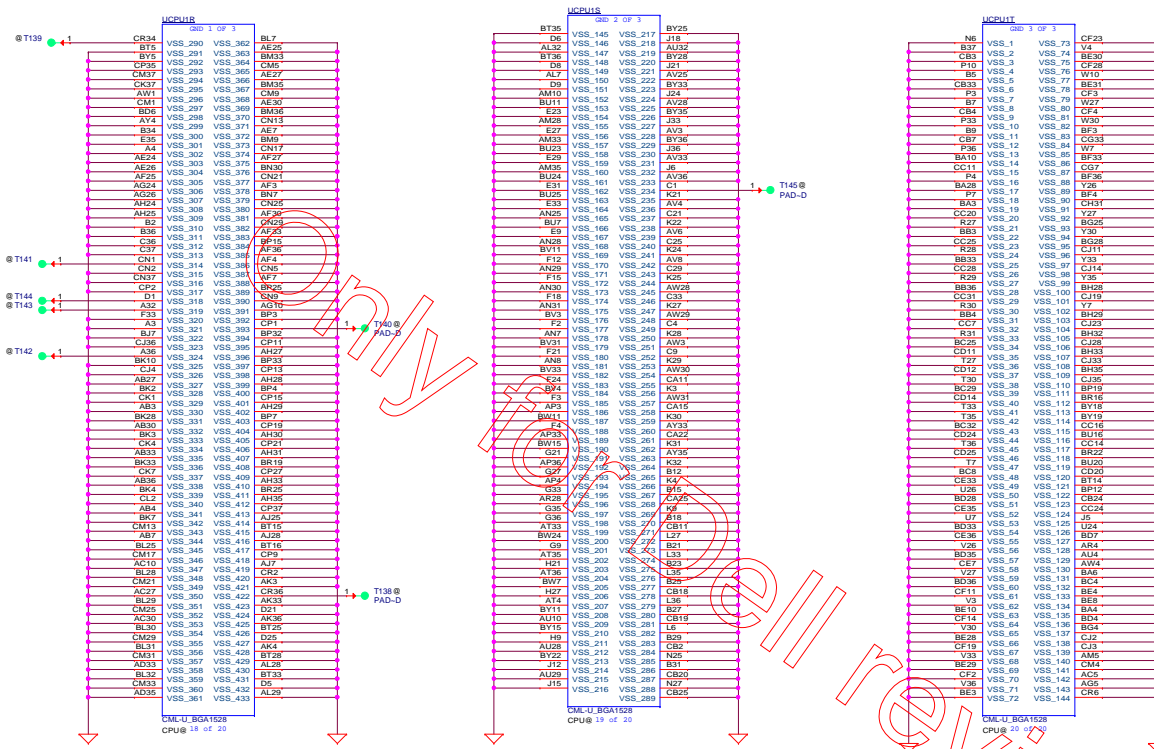
DATE	VERIFICATION, EFFECTIVE DATE, 2000	CHANGES	TO	OF	100
1					





Test pin for Corner NCTF Test(#566757)  
need place on CPU corner

Note1: VCCPRIM\_CORE Implementation with PCH CORE\_V D Recommendation



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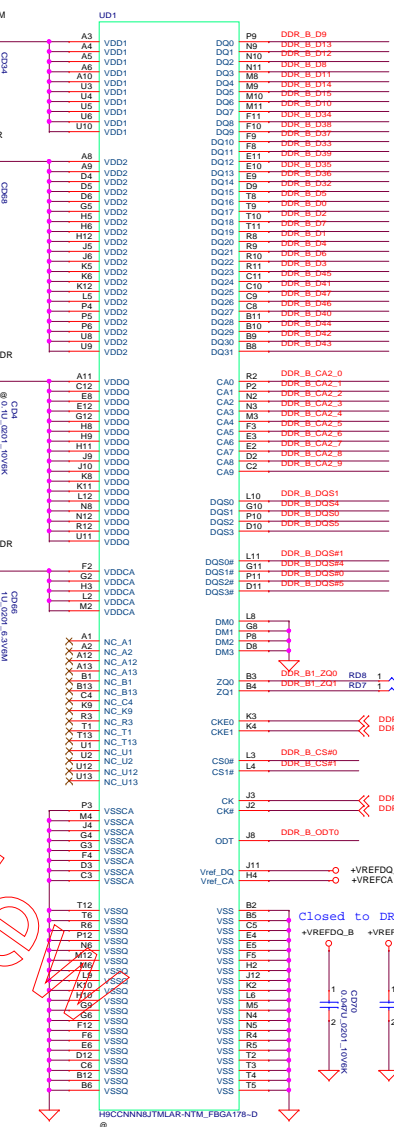
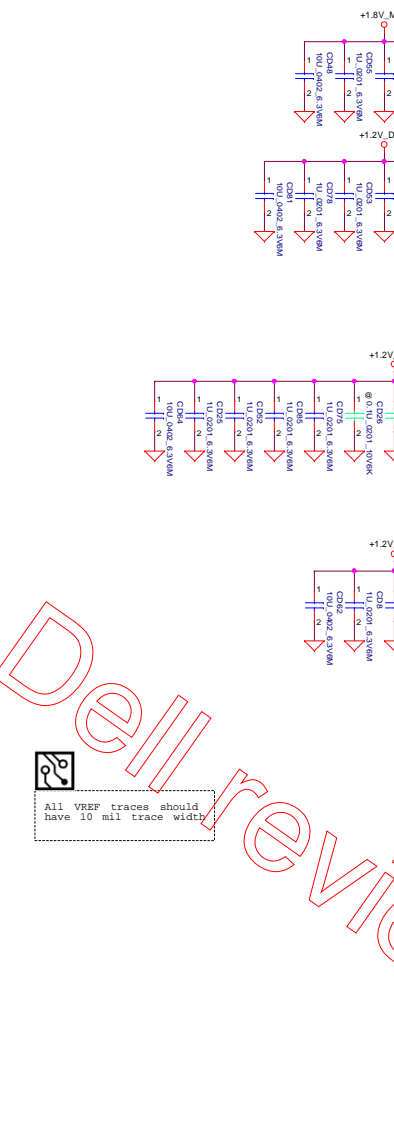
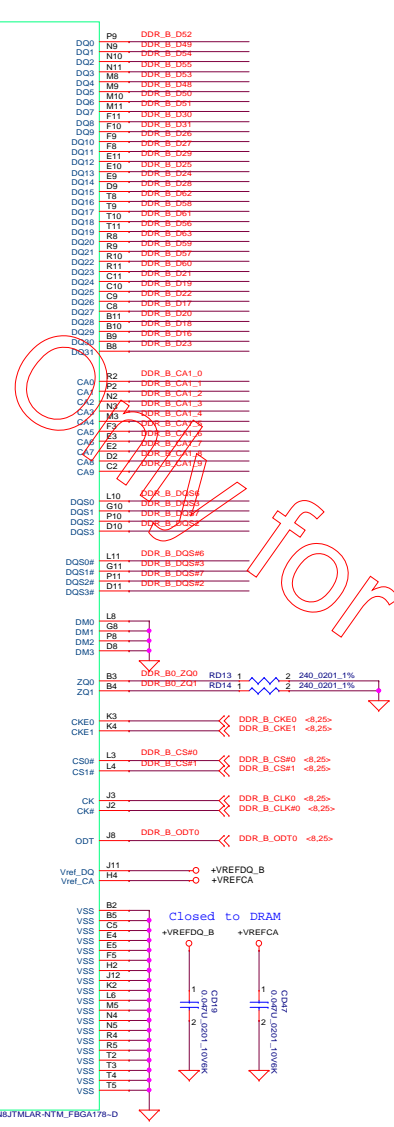
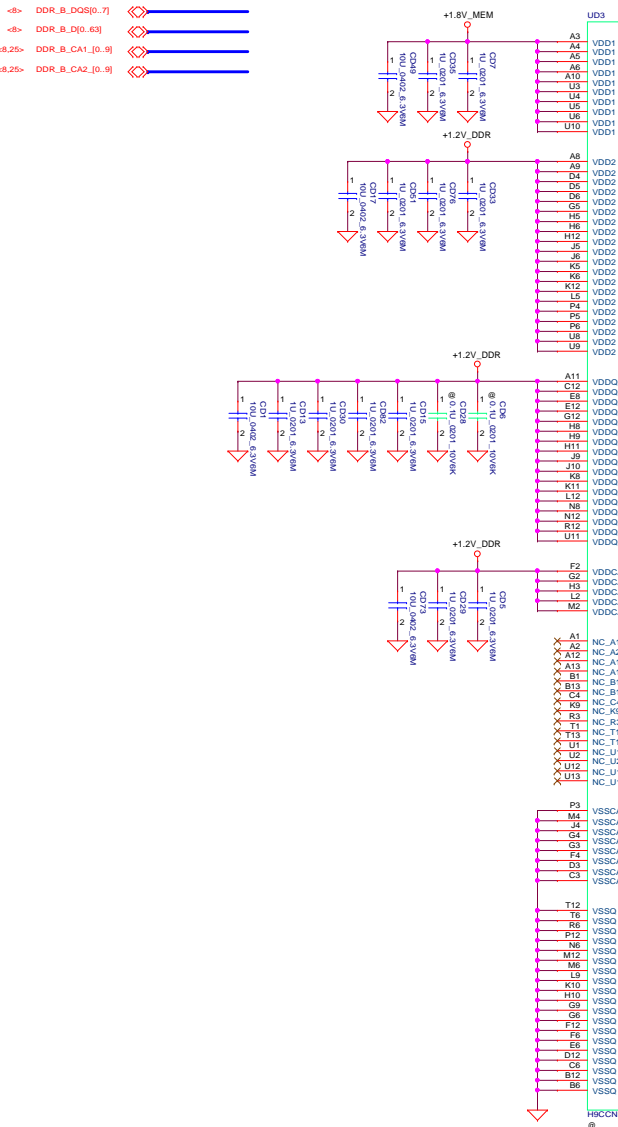
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<8> DDR\_B\_DQS[0..7]  
<8> DDR\_B\_DQS[0..7]  
<8> DDR\_B\_DQS[0..7]  
<8.25> DDR\_B\_CA1[0..9]  
<8.25> DDR\_B\_CA2[0..9]



Decoupling per DRAM device  
VDDQ 4x 0402 1uF 2x 0201 0.1uF 1x 0603 10uF  
VDDCA 2x 0402 1uF 1x 0603 10uF  
VDD2 3x 0402 1uF 1x 0603 10uF  
VDD1 2x 0402 1uF 1x 0603 10uF  
intel used 0201 for 0.1uF

All VREF traces should have 10 mil trace width

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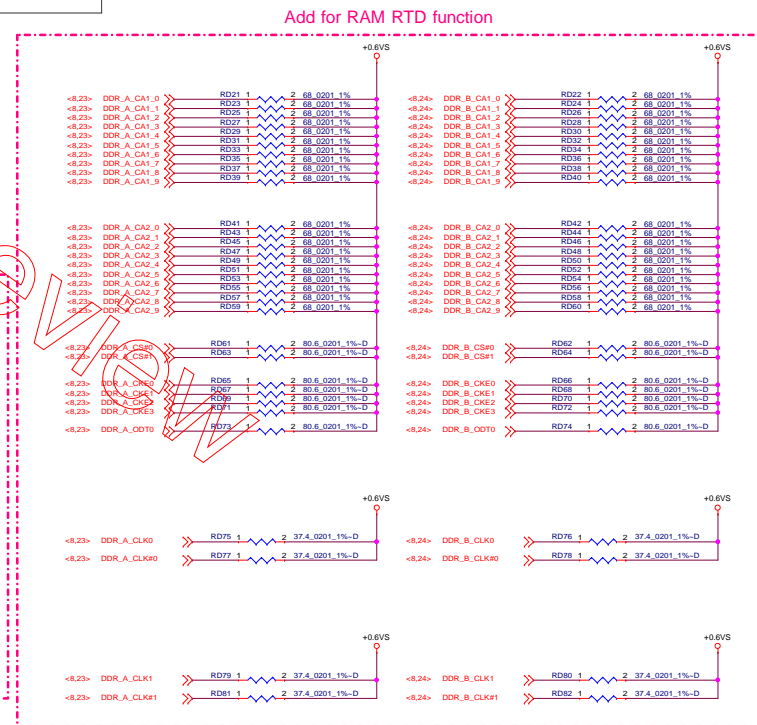
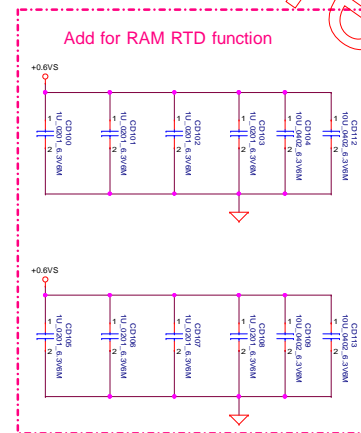
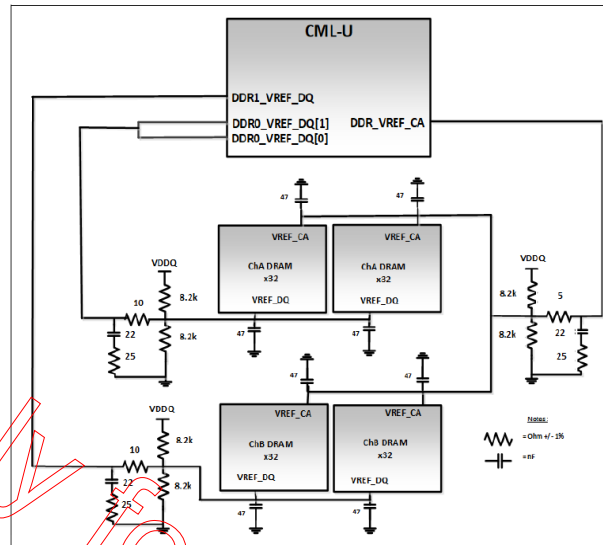
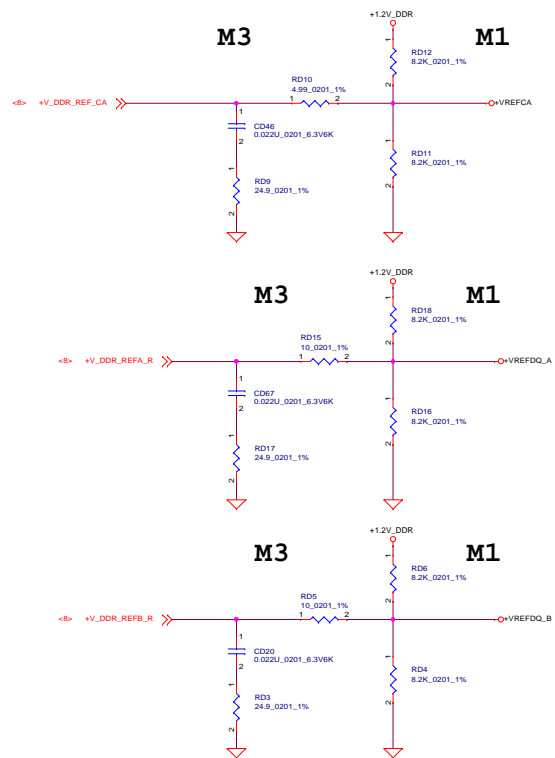
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VREF traces should be at least 20 mils wide with 20 mils spacing to other signals/planes.

Figure 60. LPDDR3 x32 Memory Down VREF-DQ and VREF-CA Overview



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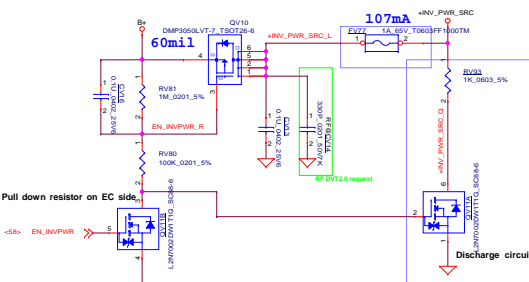
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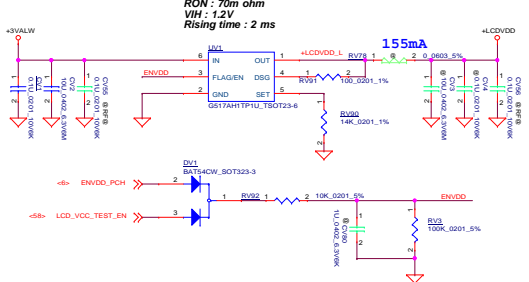
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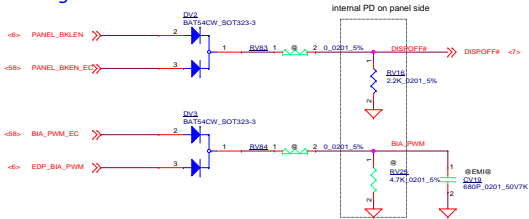
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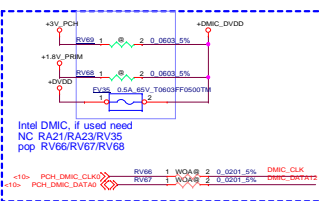
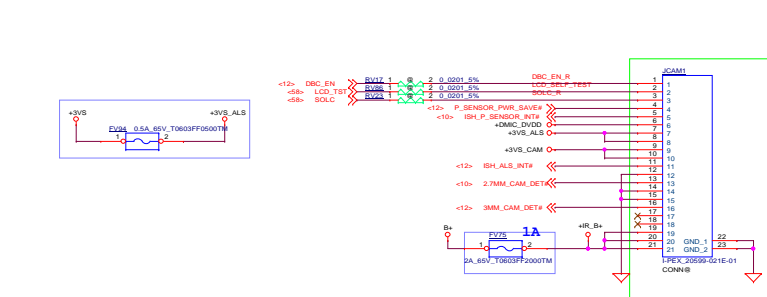
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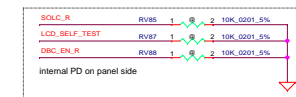
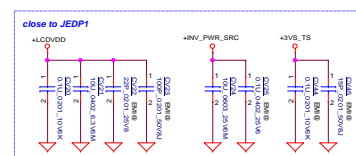
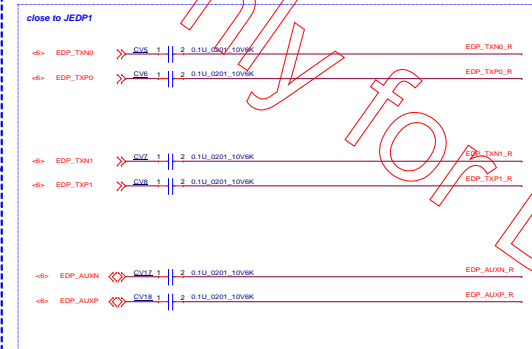
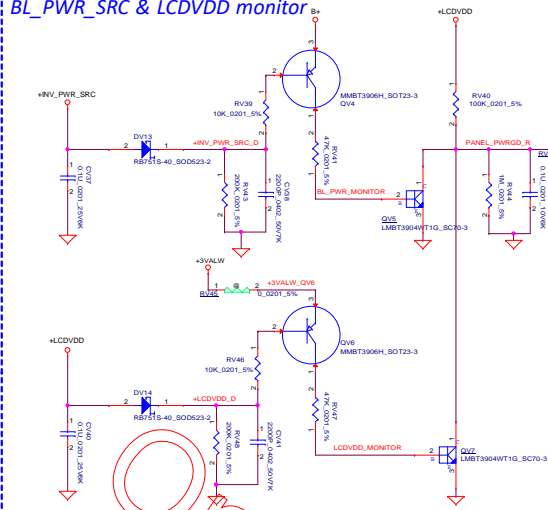
## BackLight PWM Control



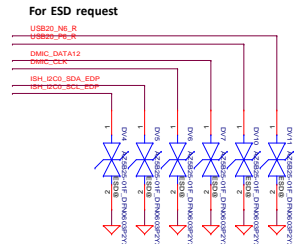
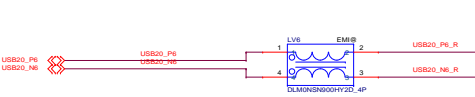
## CAM CONN



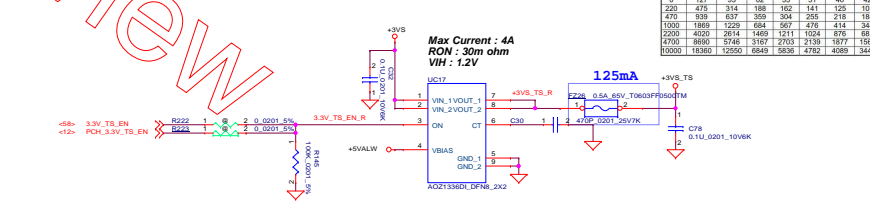
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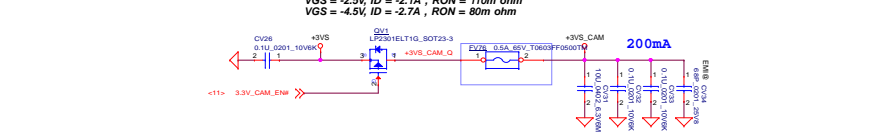
CNT	FN #	Host MEM	IO	Description	Allowable Operating Voltage (V)
1	STOP			HIGH: Normal Operation LOW: Stop Scanning Buskin pull-up (to 3.3 volts) resistor 35kOhm	V <sub>DD</sub> 0.75V <sub>DD</sub> V <sub>DD</sub>
2	IC SDA		IO	IC Data Open drain output: pull-up resistor at Host is needed	V <sub>DD</sub> 1.35 V <sub>DD</sub>
3	IC SCL		IO	IC Clock Open drain output: pull-up resistor at Host is needed	V <sub>DD</sub> 1.35 V <sub>DD</sub>
4	NC		-	No Connection	-
5	NC		-	No Connection	-
6	IC IRQ		IO	IC Data Ready Output "LOW" when data ready to send Open drain output: pull-up resistor at Host is needed	V <sub>DD</sub> 1.35 V <sub>DD</sub>
7	RESET		IO	Hardware RESET Low Active Stop operation when pull "LOW" Buskin pull-up (to 3.3 volts) resistor 10kOhm	V <sub>DD</sub> 0 0.4
8	VDD +3.3V		-	3.3 volt (typ) power input	3.14 3.45
9	NC		-	No Connection	-
10	DSND		-	Ground	-



## 3VS\_TS



## 3VS\_CAM



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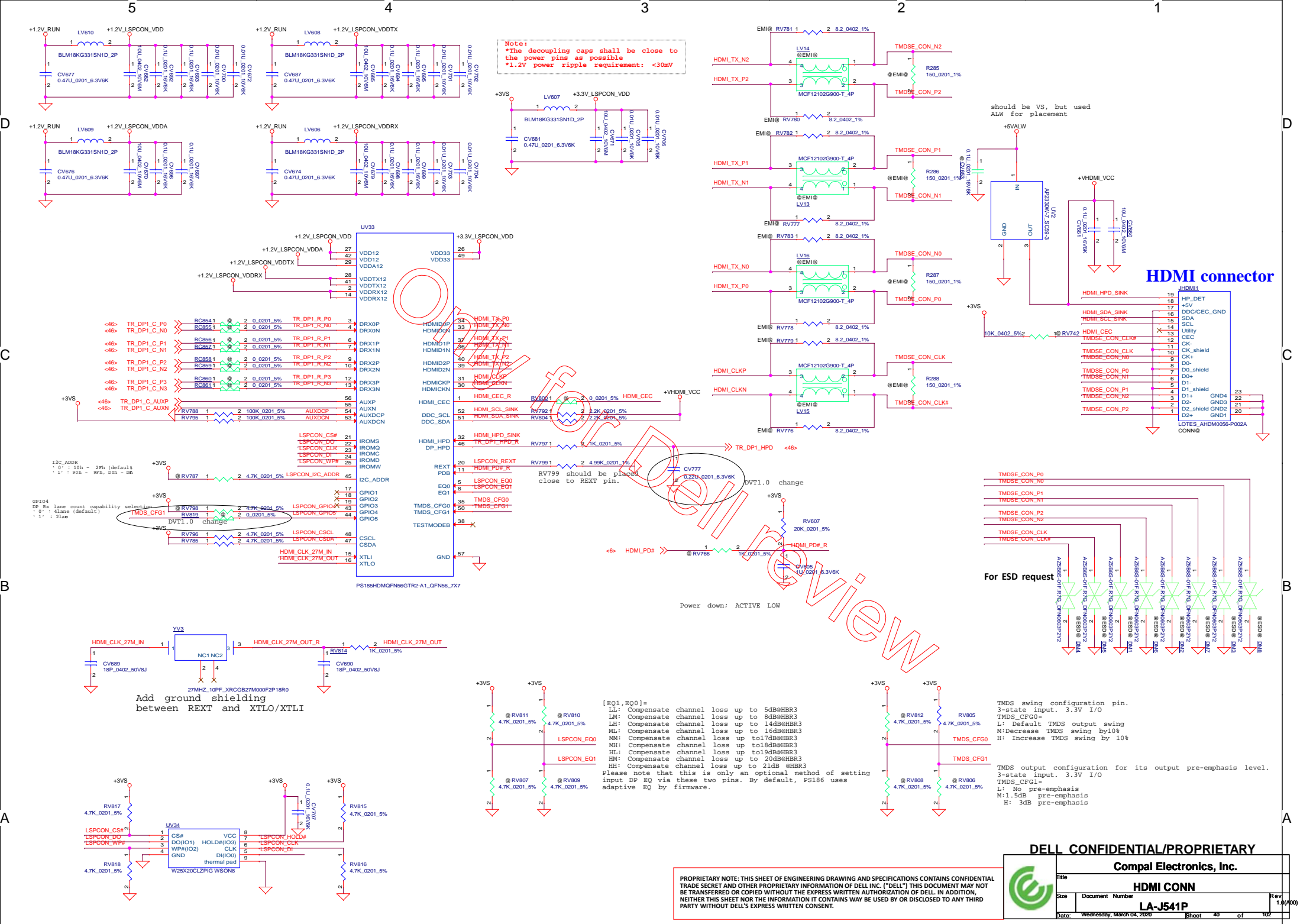
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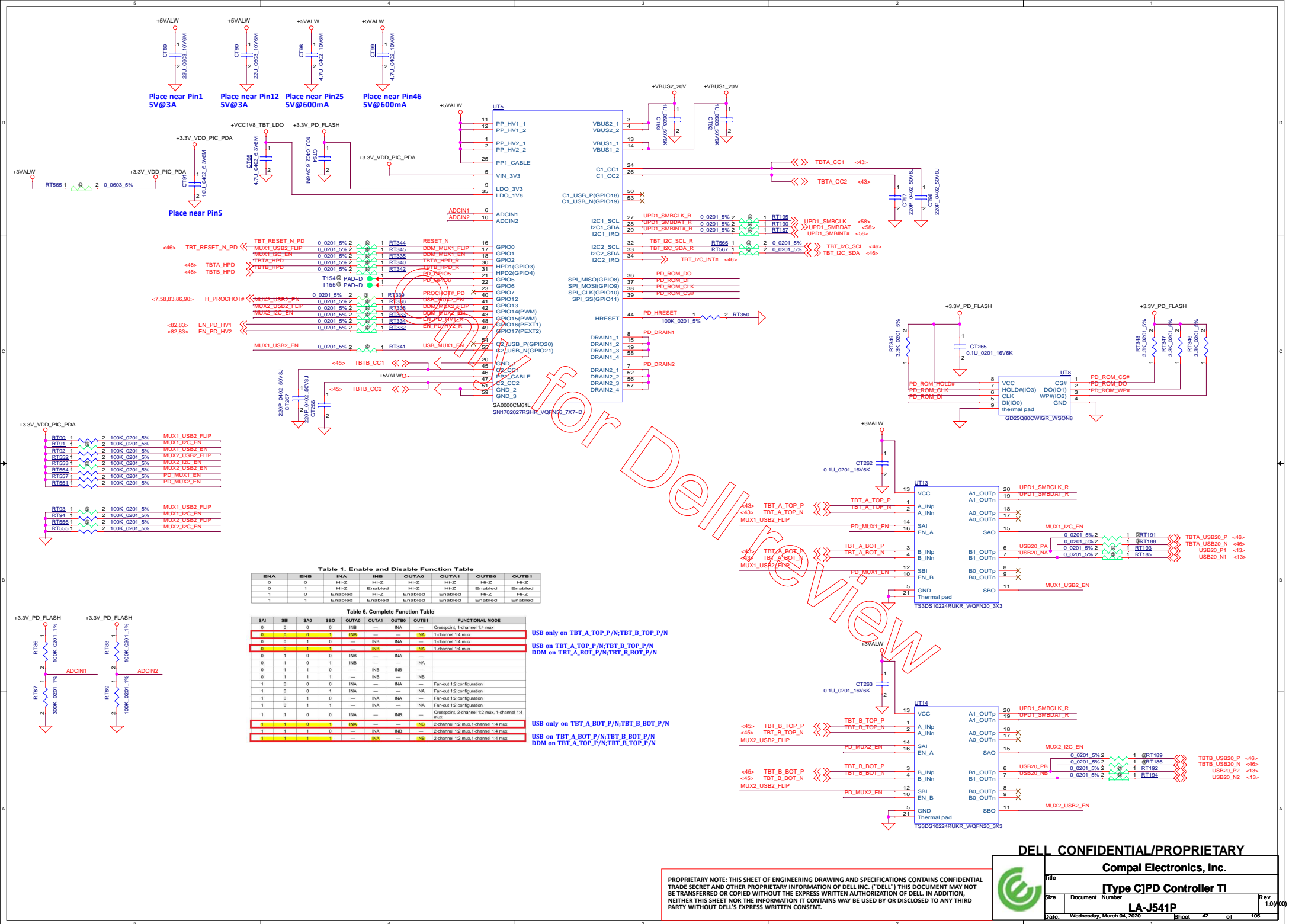
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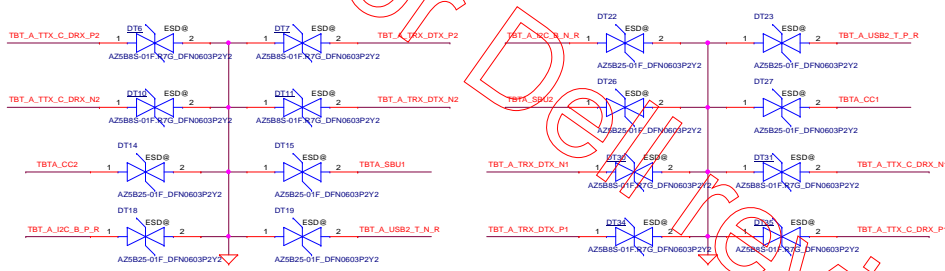
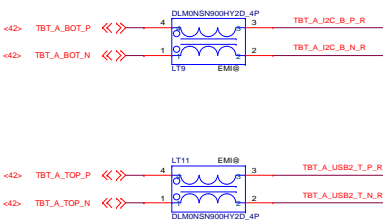
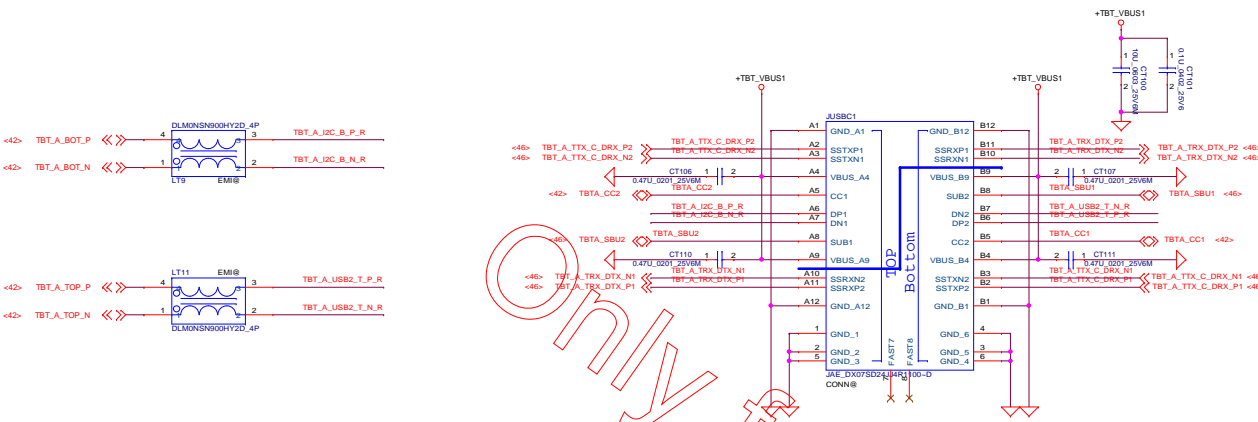
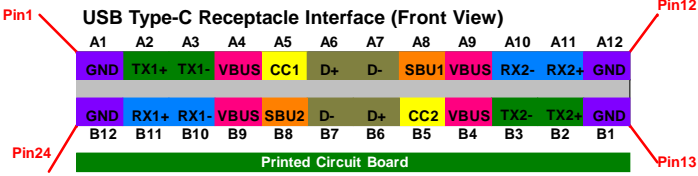
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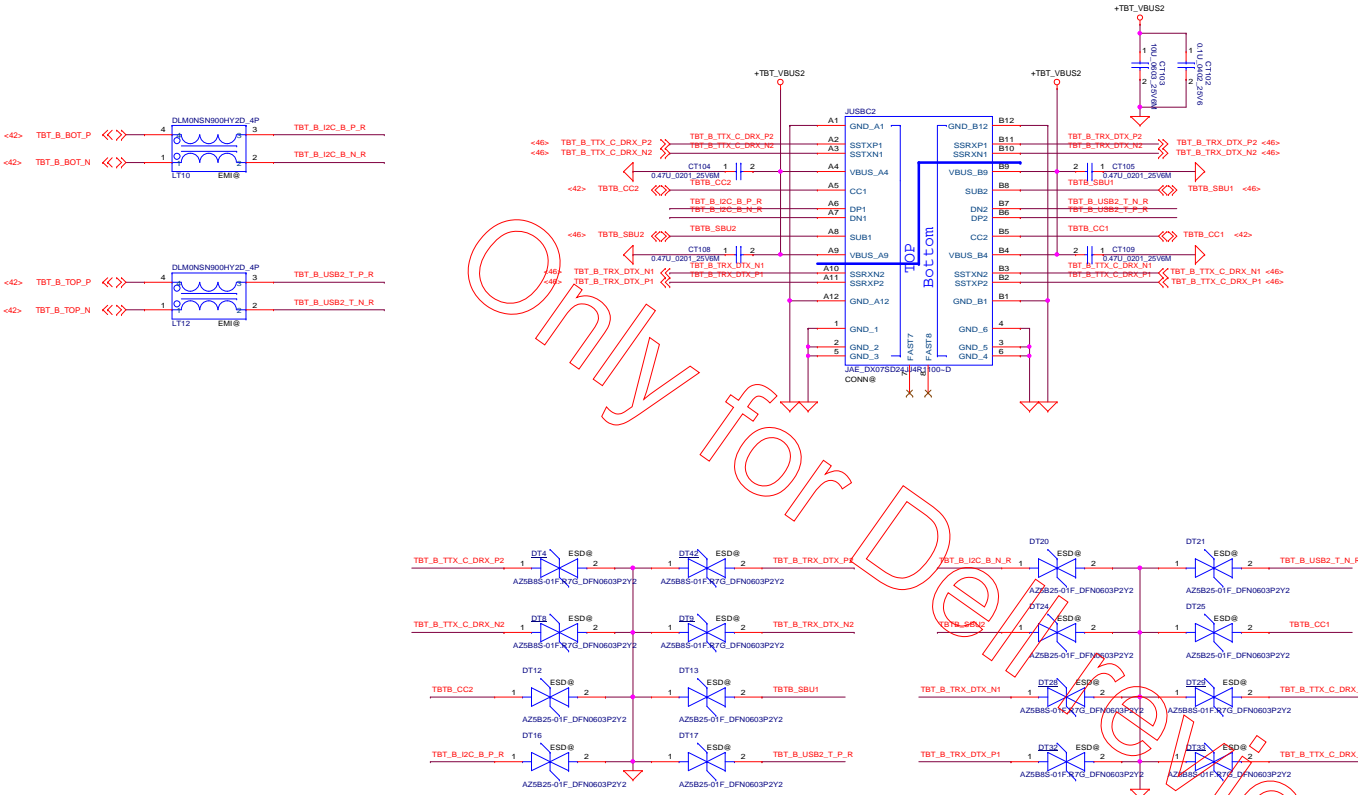
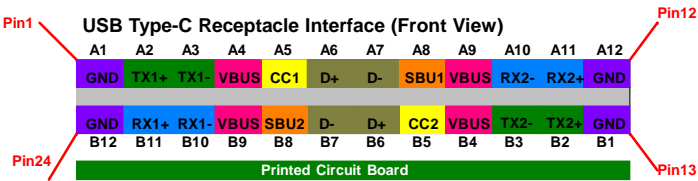
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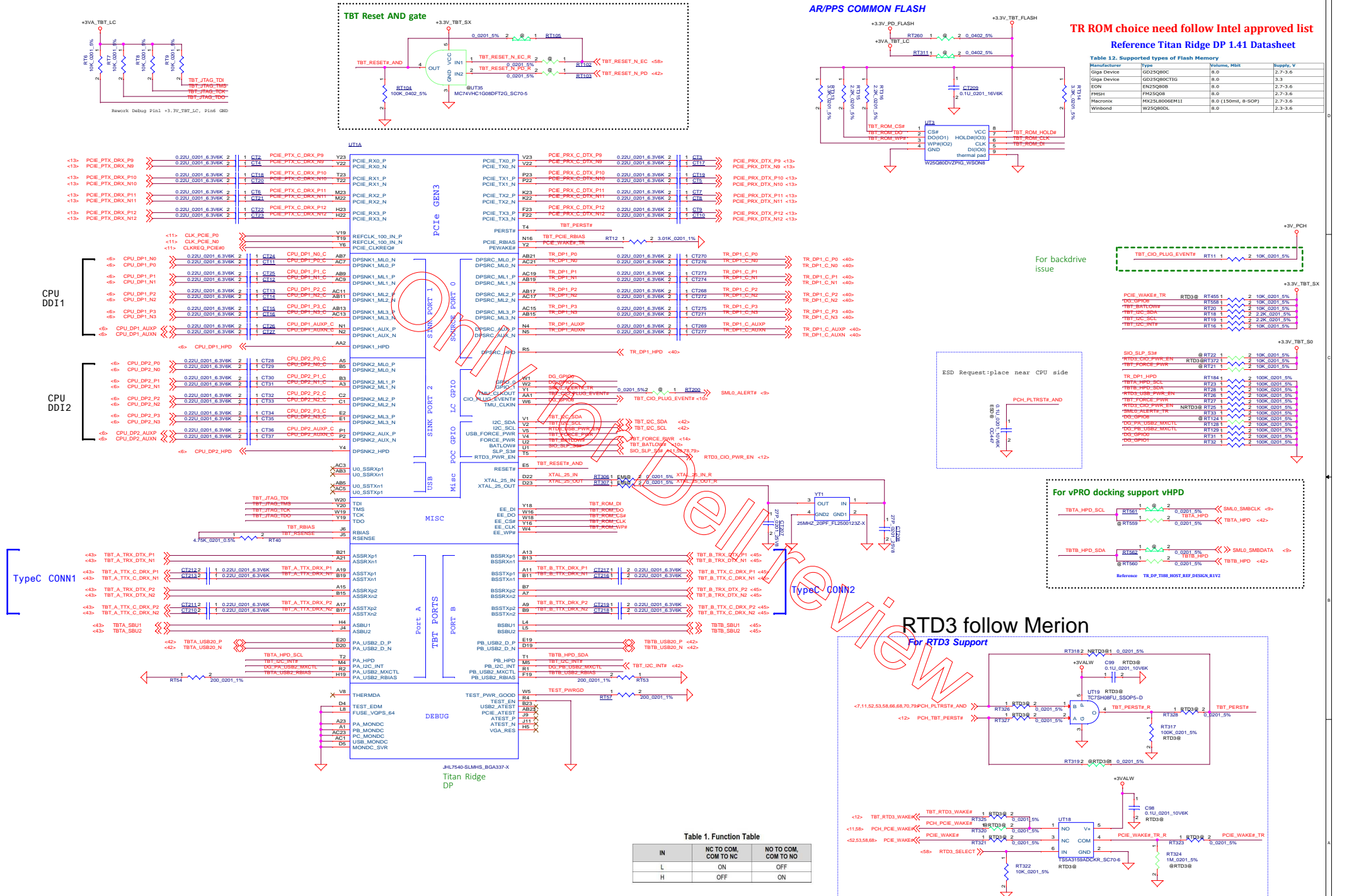


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				Rev 1.0/400	
Date: Wednesday, March 04, 2020				Sheet 44 of 100	

# Type-C Port-B



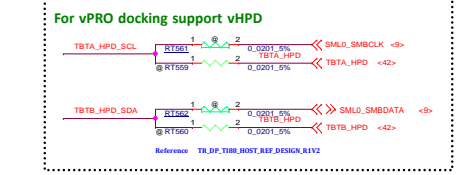


### TR ROM choice need follow Intel approved list

Reference Titan Ridge DP 1.41 Datasheet

Table 13. Supported types of Flash Memory				
Manufacturer	Type	Volume, Mbit	Supply, V	
Giga Device	GD25Q64	8.0	2.7-3.6	
Giga Device	GD25Q64CTIG	8.0	3.3	
ECW	DN25Q64	8.0	2.7-3.6	
PM95	PM25Q64	8.0	2.7-3.6	
Macronix	MX25LD064M11	8.0 (150mL, 8-SOP)	2.7-3.6	
Winbond	W25Q64DL	8.0	2.3-3.6	

For backdrive issue



### RTD3 follow Merion

For RTD3 Support

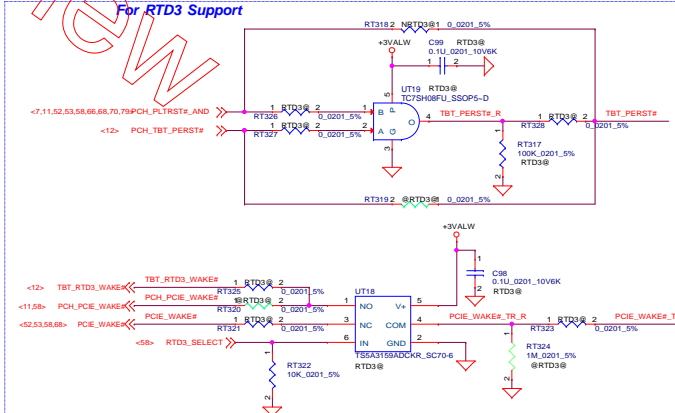
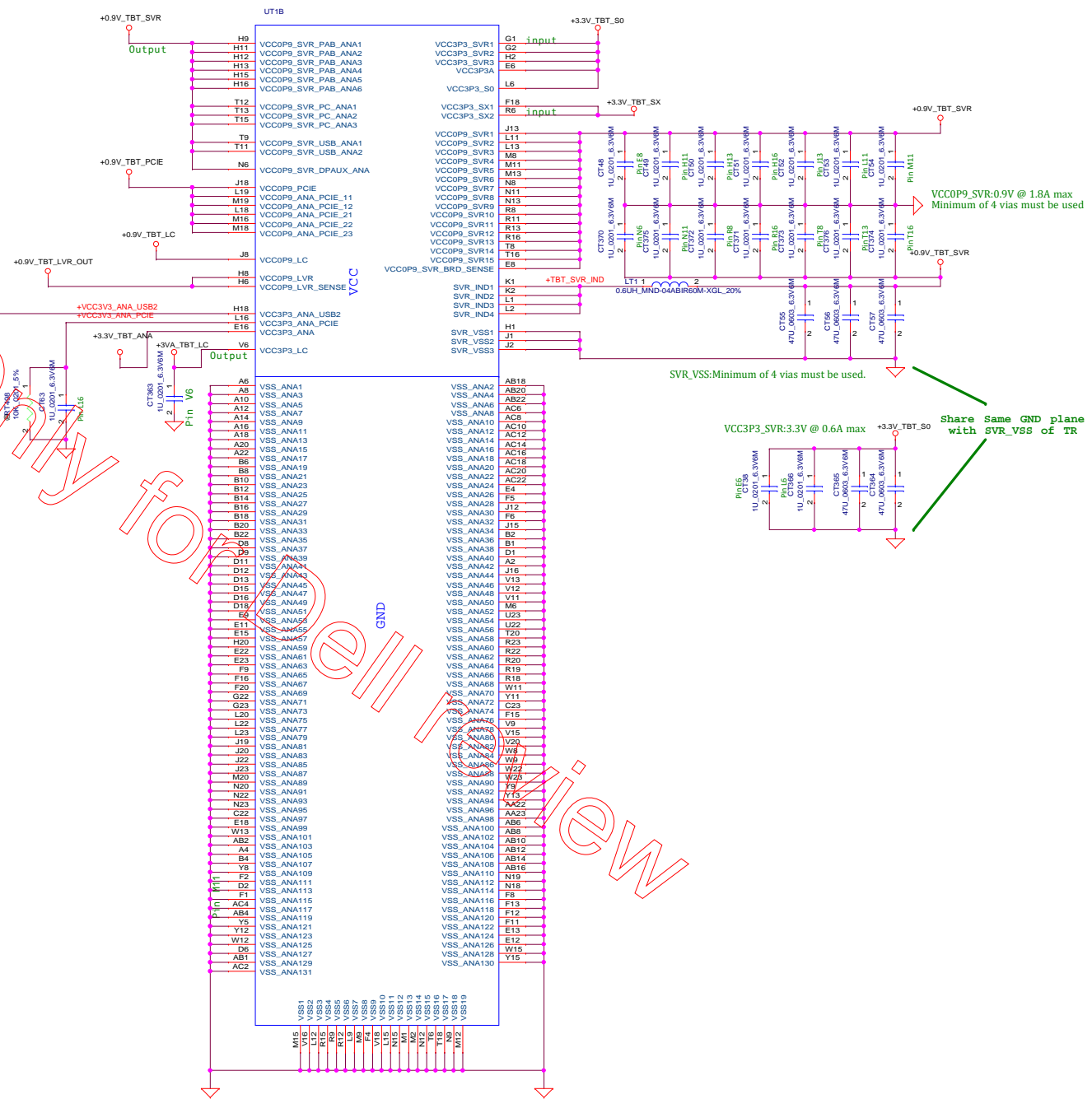
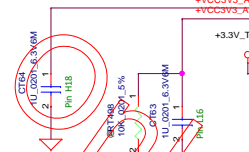
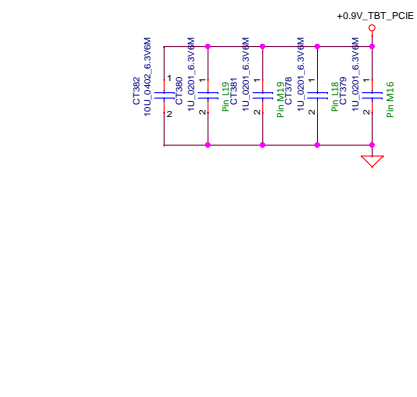
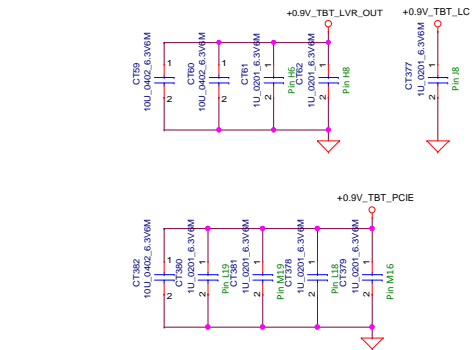


Table 1. Function Table		
IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON



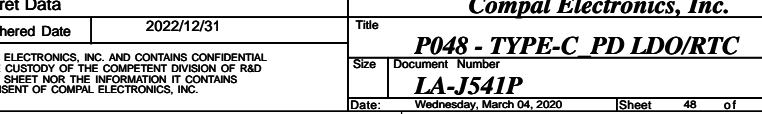
VCC3P3\_SVR:3.3V @ 0.6A max +3.3V\_T

SVR\_VSS:Minimum of 4 vias must be used.

BT\_S0      Share Same GND plane  
              with SVR\_VSS of TR

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								Date		Wednesday, March 04, 2020	
								Sheet		47 of 105	

5	4	3
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3	2	1
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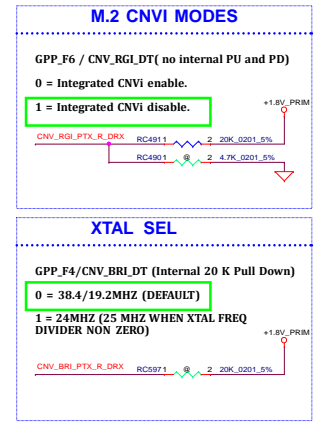
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		1.0(A00)			
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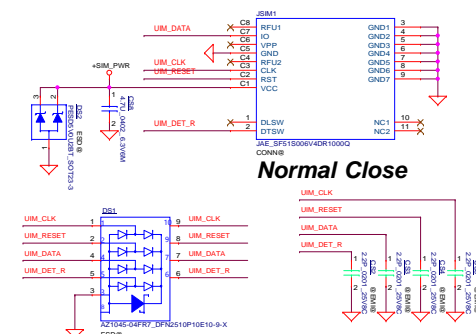
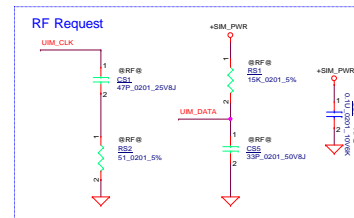
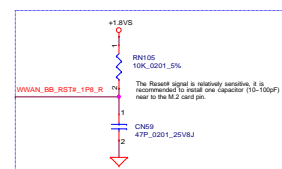
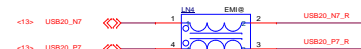
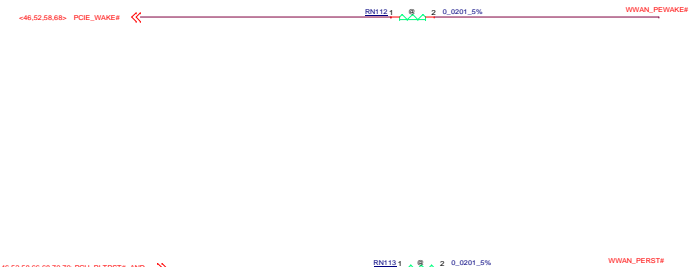
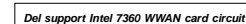
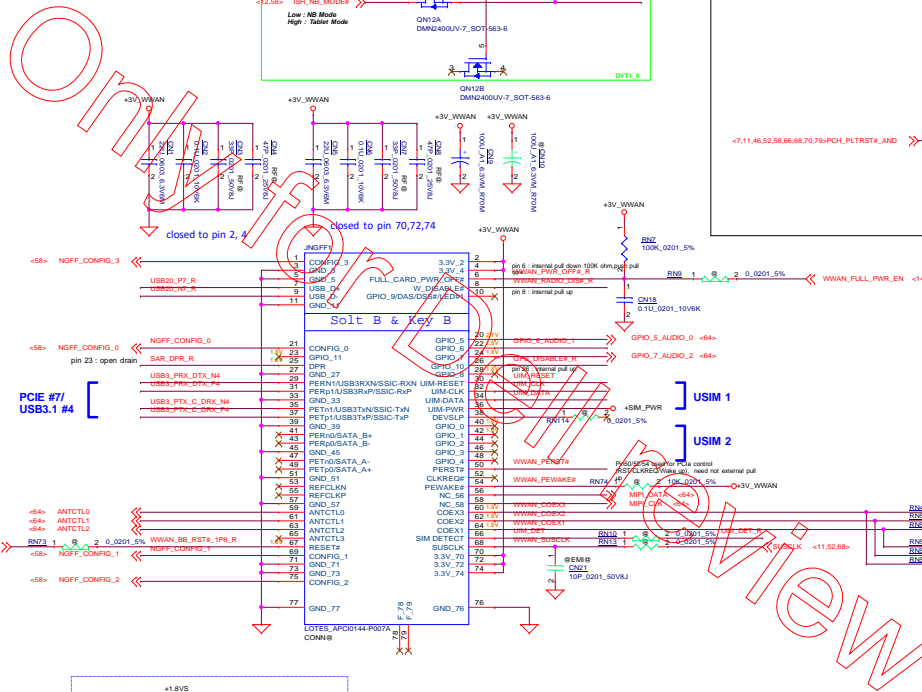
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Size Document Number <b>LA-J541P</b>				Date: Wednesday, March 04, 2020 Sheet 62 of 100	

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## Del PCIe/USB 3.0 Mux

## USB 3.1 #4

<13>	USB3_PTX_DRX_P4	1	2	0.1U_0201_10V6K	USB3_PTX_C_DRX_P4
<13>	USB3_PTX_DRX_N4	1	2	0.1U_0201_10V6K	USB3_PTX_C_DRX_N4
<13>	USB3_PRX_DTX_P4				USB3_PRX_C_DTX_P4
<13>	USB3_PRX_DTX_N4				USB3_PRX_C_DTX_N4

TABLE 2  
CIRCUIT DETECTION SWITCH AND DELAY SWITCH

	WITHOUT TRAY	TRAY MATED
DETECTION SWITCH		

## uSIM CONN

State#	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module	Type	Port	Configuration
0	GND	GND	GND	GND	SSD	SATA	N/A	
1	GND	HIGH	GND	GND	SSD	PCIe	N/A	
2	GND	GND	HIGH	GND	WWAN	PCIe	0	
3	GND	HIGH	HIGH	GND	WWAN	PCIe	1	
4	GND	GND	GND	HIGH	WWAN	USB 3.0	0	
5	GND	HIGH	GND	HIGH	WWAN	USB 3.0	1	
6	GND	GND	HIGH	HIGH	WWAN	USB 3.0	2	
7	GND	HIGH	HIGH	HIGH	WWAN	USB 3.0	3	
8	HIGH	GND	GND	GND	WWAN	SSIC	0	
9	HIGH	HIGH	GND	GND	WWAN	SSIC	1	
10	HIGH	GND	HIGH	GND	WWAN	SSIC	2	
11	HIGH	HIGH	HIGH	GND	WWAN	SSIC	3	
12	HIGH	GND	GND	HIGH	WWAN	PCIe	2	
13	HIGH	HIGH	GND	HIGH	WWAN	PCIe	3	
14	HIGH	GND	HIGH	HIGH	DDP HCA	PCIe	N/A	
15	HIGH	HIGH	HIGH	HIGH	No Module		N/A	

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			Size Document Number <b>LA-7541P</b>	
			Date: 2020/04/20 Sheet 43 of 100 Rev 1.0/100	

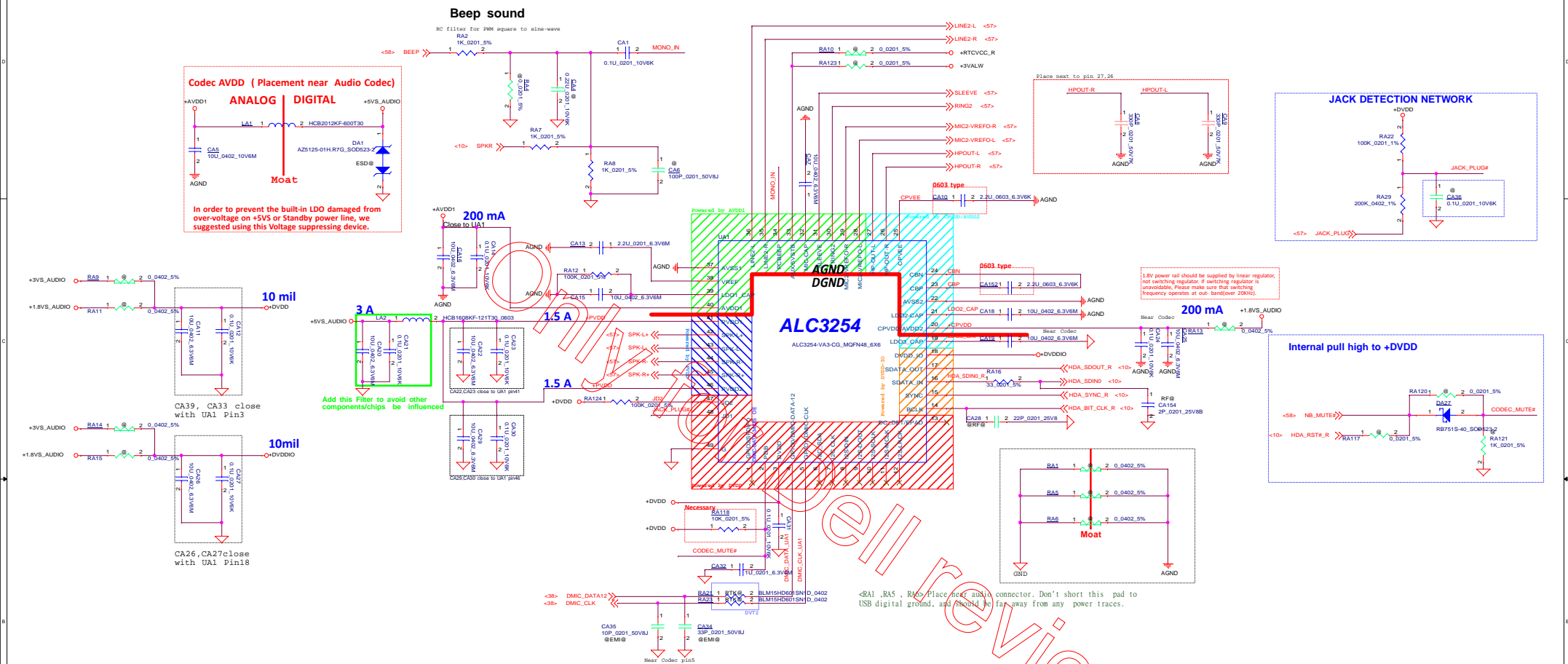
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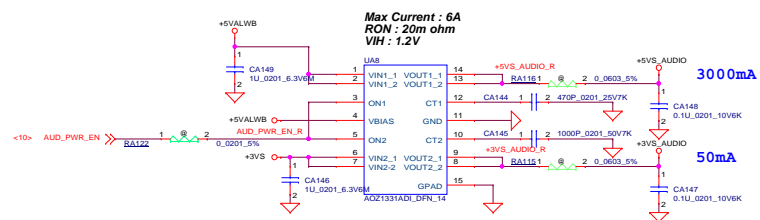
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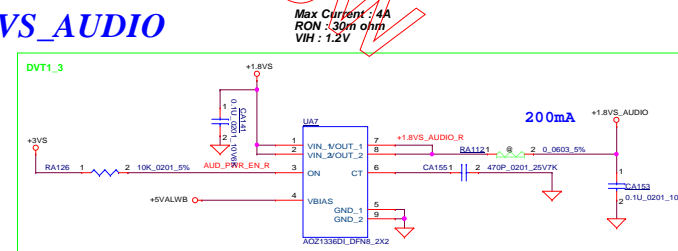


## 5VS\_AUDIO & 3VS\_AUDIO



C <sub>TX</sub> (pF)	Rise Time (μs) 10%~90%, C <sub>IN</sub> =0.1μF, C <sub>RK</sub> =1μF, R <sub>OX</sub> =10Ω							
	Typical Values at 25°C, 25V 17R 10Ω Ceramic Cap.							
	V <sub>IN</sub> =5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V	
0	85	68	49	45	40	37	34	
220	431	297	172	147	122	106	89	
470	888	583	332	269	218	189	161	
1000	1700	1130	657	550	446	390	316	
2200	3805	2534	1347	1152	966	867	701	
4700	8053	5255	1997	2578	2101	1838	1483	
10000	18330	12050	5545	5545	4155	4155	3393	

## 1.8VS\_AUDIO

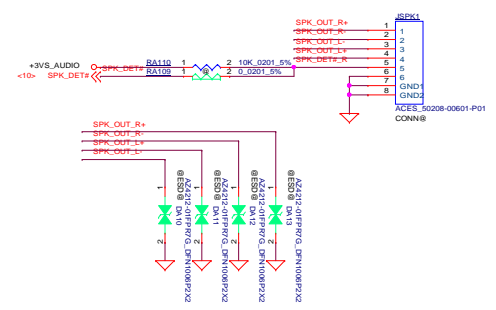
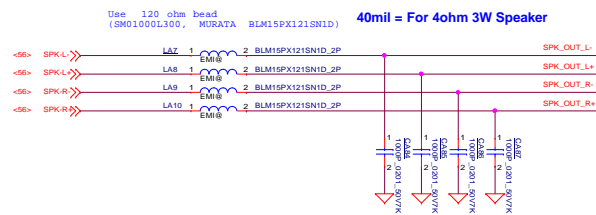


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			Date:	Wednesday, April 04, 2020
			Sheet	56 of 100



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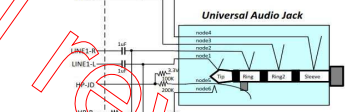
## Int. Speaker Conn.



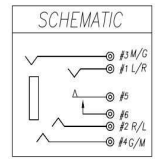
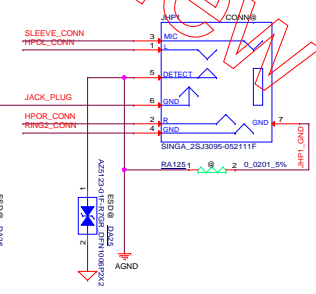
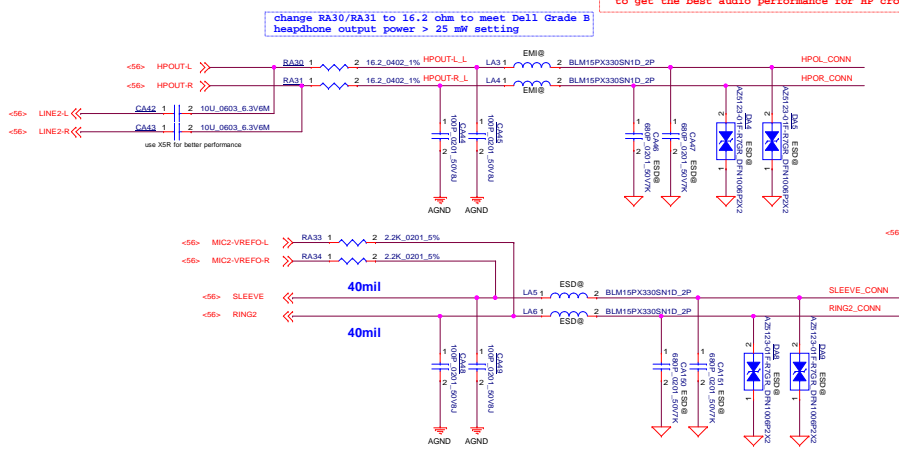
## Universal Audio Jack

## Analog Connector and Device

PCB trace width of MIC2-S(SLEEVE)/MIC2-L(RING2) are required at least 40 mil for HP crosstalk consideration and, its length should be as short as possible.  
LA19/L15 should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk.

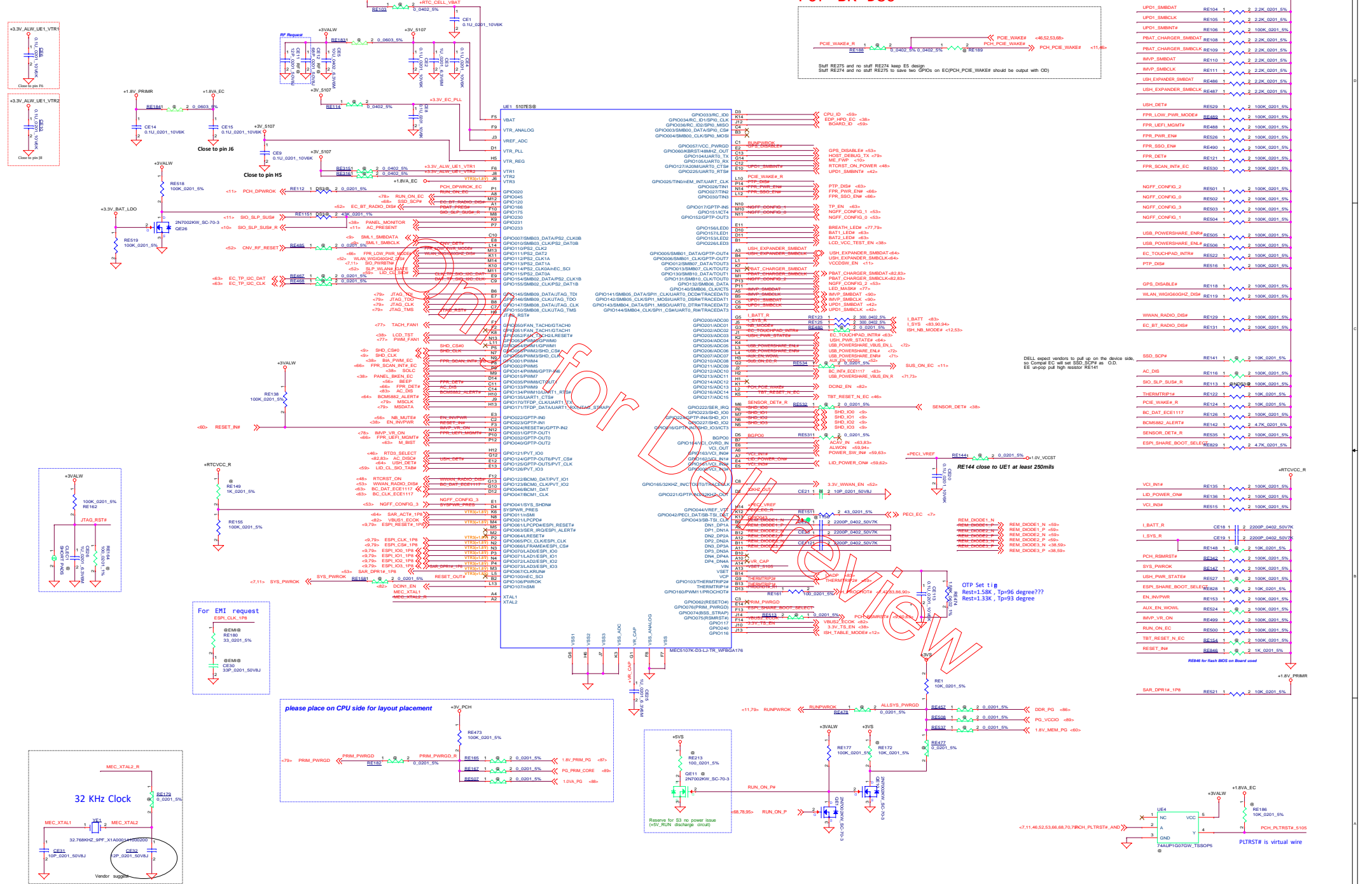


## Universal Audio Jack CONN

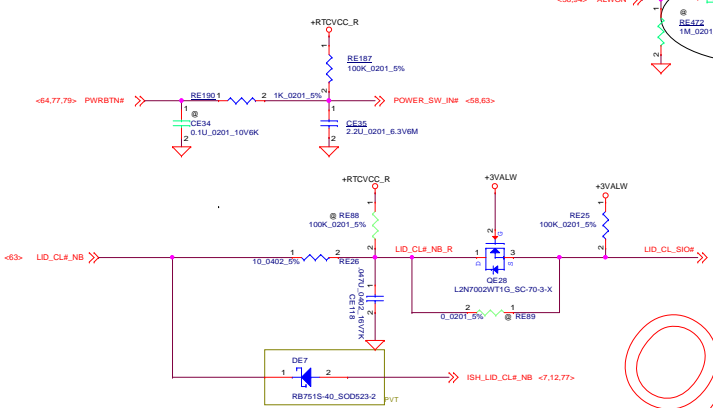


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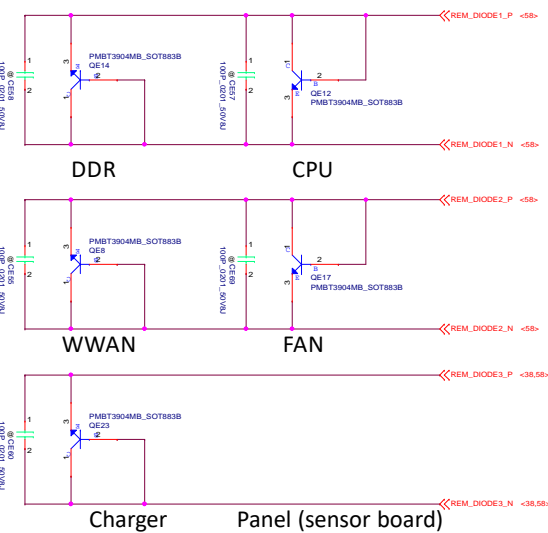
For BR DSC



Power SW / NB\_LID



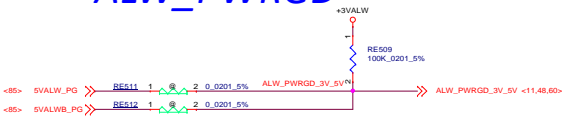
Thermal



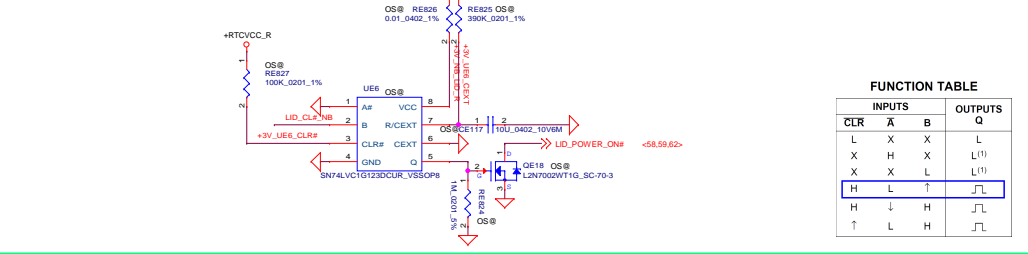
Thermal diode mapping

MECS105 pins	thermal diode	Location
DP1/DN1	QE12	CPU(OTP,Tp=96)
DN1a/DP1a	QE14	DDR
DP2/DN2	QE17	FAN
DN2a/DP2a	QE8	WWAN
DP3/DN3	QE24	Panel (sensor board)
DN3a/DP3a	QE23	Charger
DP4/DN4	QE22	NC
DN4a/DP4a	QE25	NC

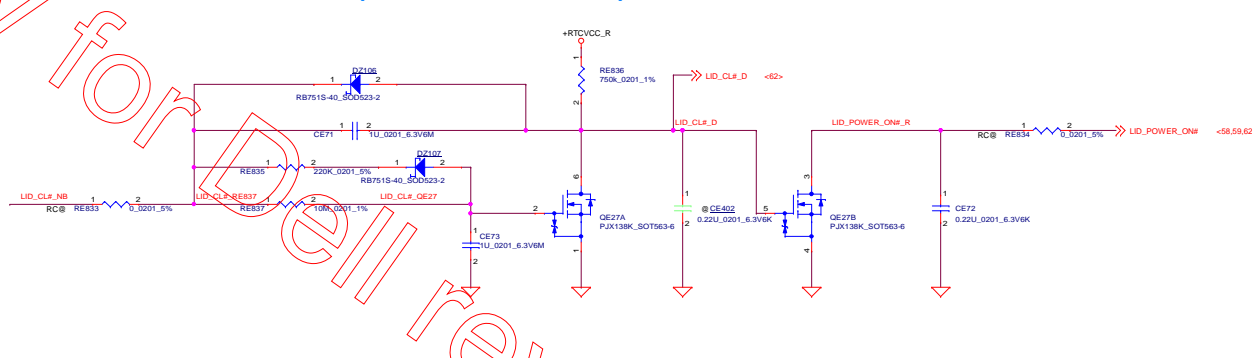
ALW\_PWRGD



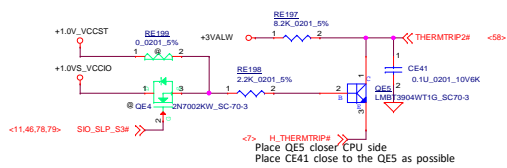
S5 LID OPEN POWER ON



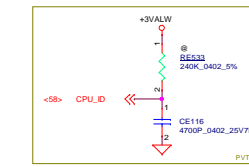
S5 LID OPEN POWER ON(Other Solution)



Board ID



RE200	CE44	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
4.3K	4700p	A00
2K	4700p	
1K	4700p	

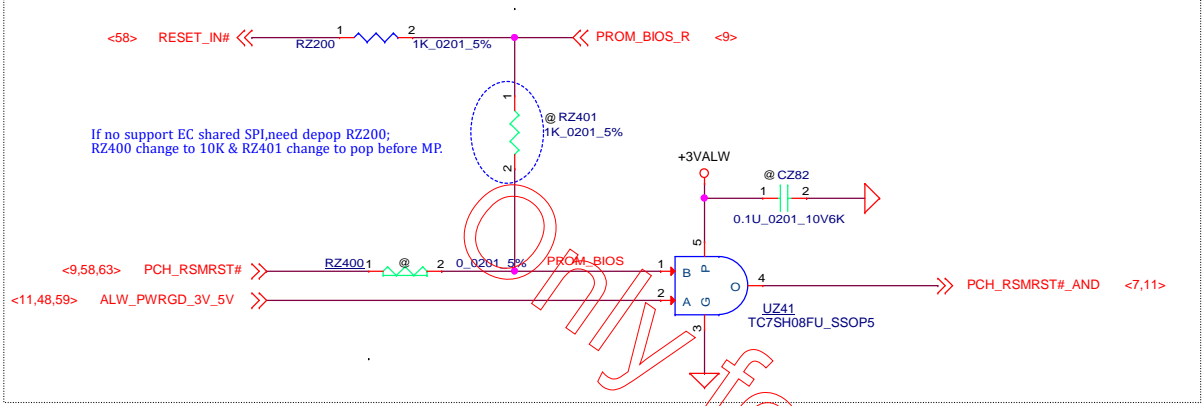


RE533	CE116	REV
240K	4700p	V-PRO I5
130K	4700p	V-PRO I7
62K	4700p	Non V-PRO I5
33K	4700p	Non V-PRO I7
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

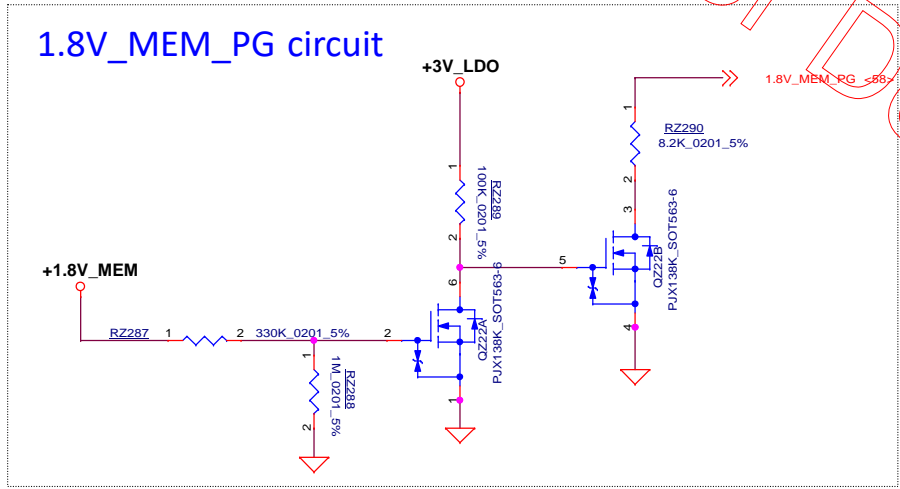
BOARD\_ID rise time is measured from 5%~68%

CPU\_ID rise time is measured from 5%~68%

RSMRST circuit



1.8V\_MEM\_PG circuit

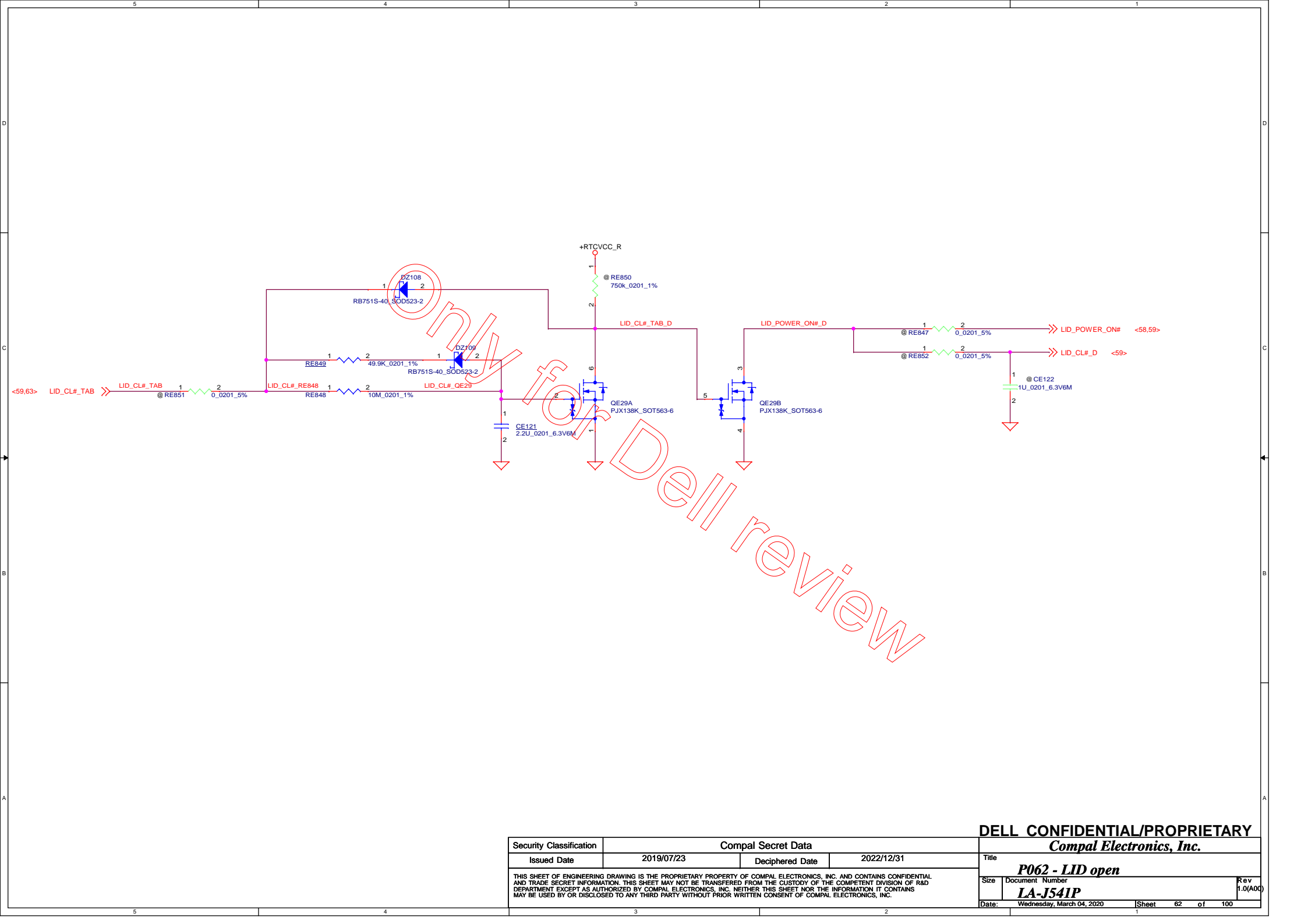


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				Sheet	60 of 100
				Rev	1.0(A00)

CML-U

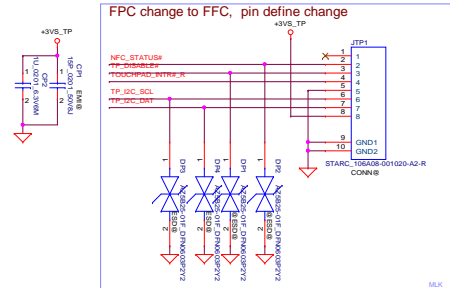
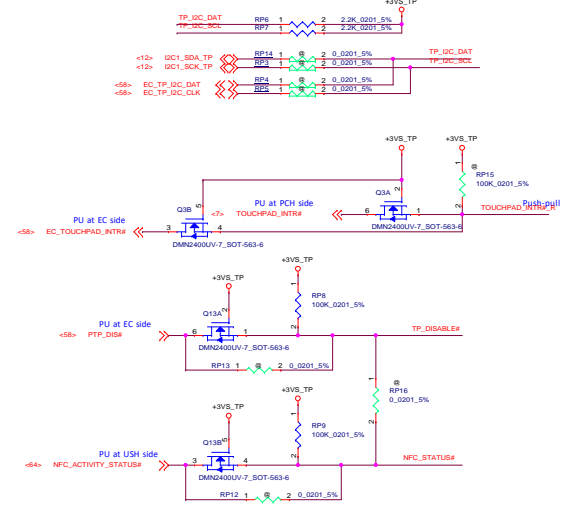
KBC  
MEC 5107

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2016/07/23		2022/12/31		P061 - SMR/I2C Block Diagram	
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LA-J541P		1.0		1.0	
DATE		DESIGN		BY	



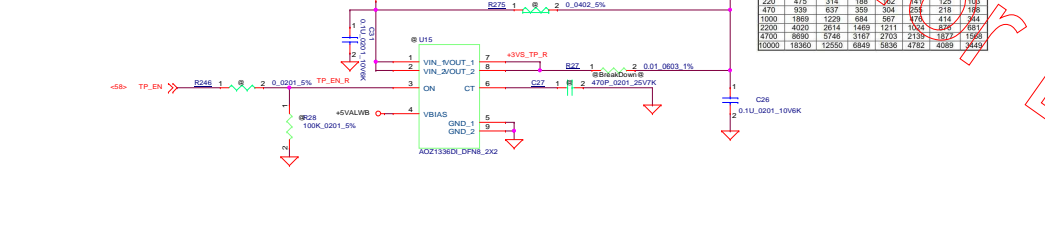
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Deciphered Date		2022/12/31		Title	
				P062 - LID open	
				Size	
				Document Number	
				LA-J541P	
				Date	
				Wednesday, March 04, 2020	
				Sheet	
				62 of 100	
				Rev	
				1.0(A00)	

Touch Pad CONN

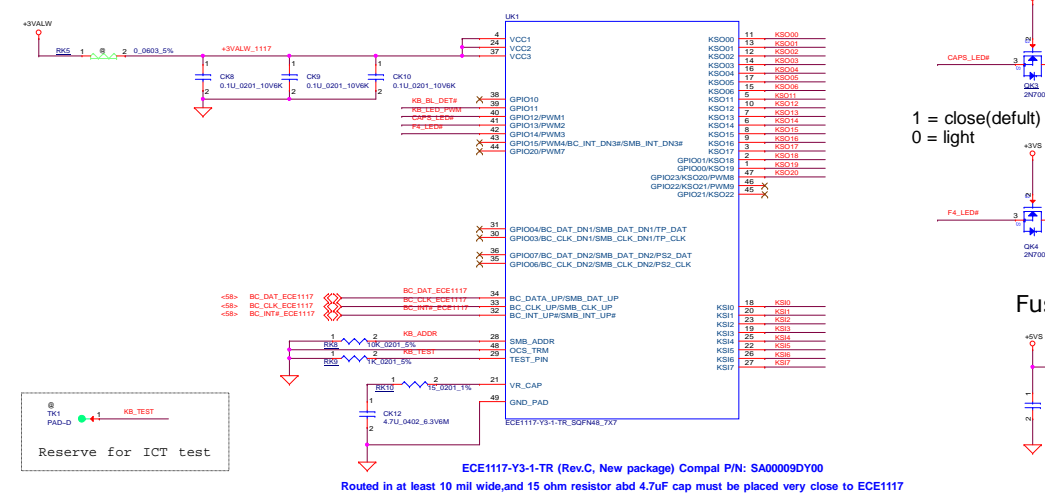


Pin No.	Definition	Description
1	Vdd (+3.3V D.C)	3.3V D.C
2	I2C SDA	Bidirectional, open drain without pull-up
3	I2C SCL	Bidirectional, open drain without pull-up
4	GND	Signal ground
5	I2C Int.	Output, push-pull
6	Disable#	refer behavioral spec in later page
7	(P5/2 DATA) NFC Status	refer behavioral spec in later page
8	(P5/2 CLK) N.C	No connection
9	NFC-signal	refer behavioral spec in later page
10	N.C	

3VS\_TP

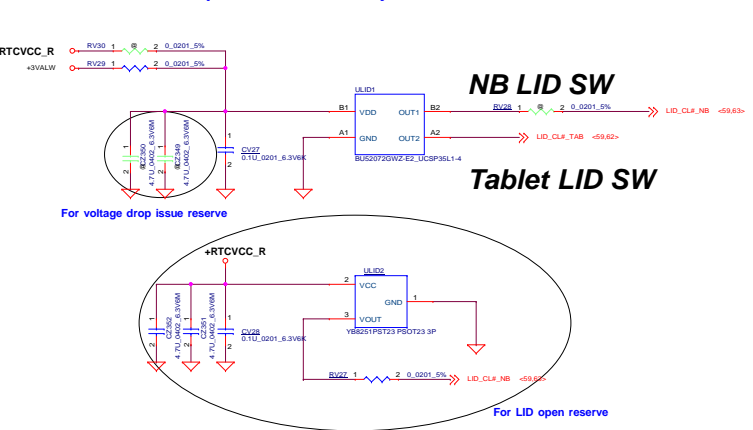


KB control & KB conn & Backlight

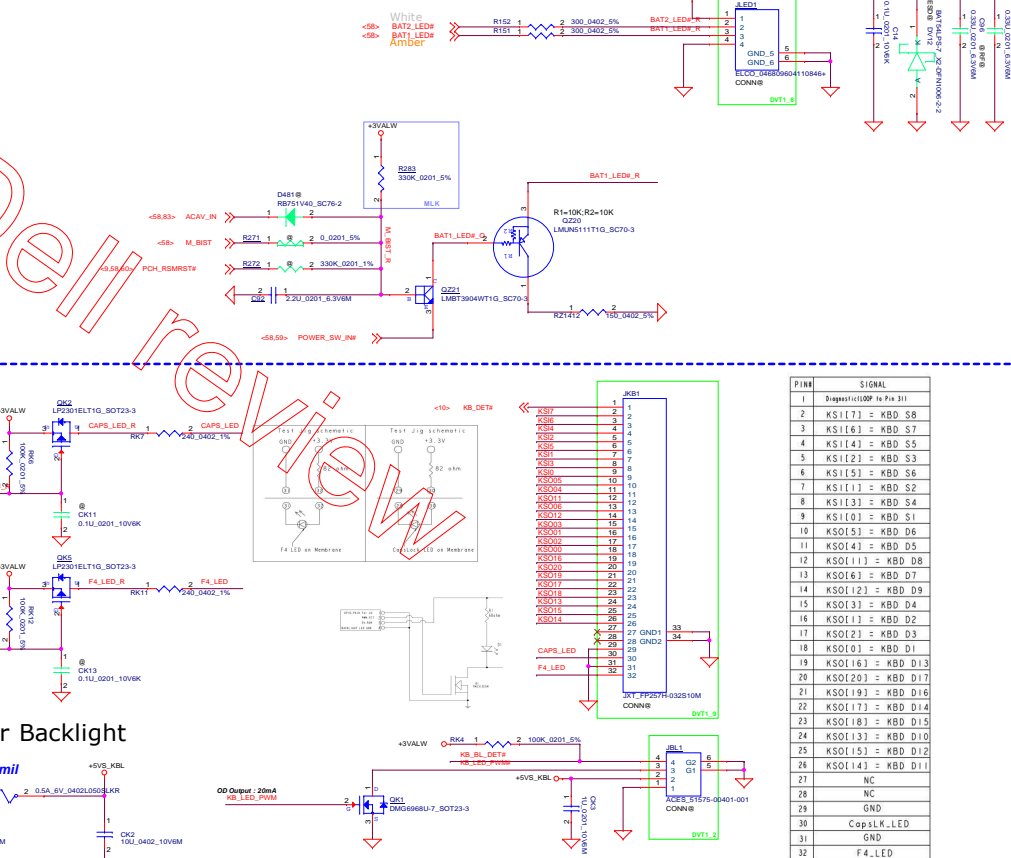


ECE1117-Y3-1-TR (Rev.C, New package) Compal P/N: SA00009D00  
Routed in at least 10 mil wide, and 15 ohm resistor abd 4.7uF cap must be placed very close to ECE1117

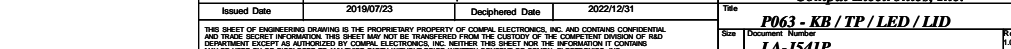
Hall Sensor (LID switch)



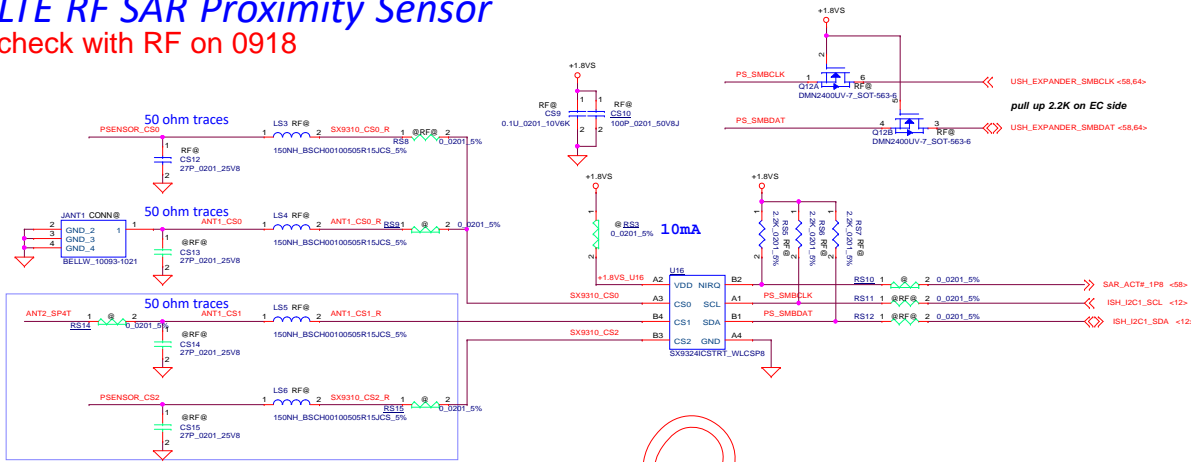
LED board



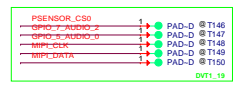
Fuse for Backlight



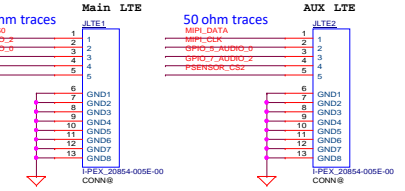
LTE RF SAR Proximity Sensor  
check with RF on 0918



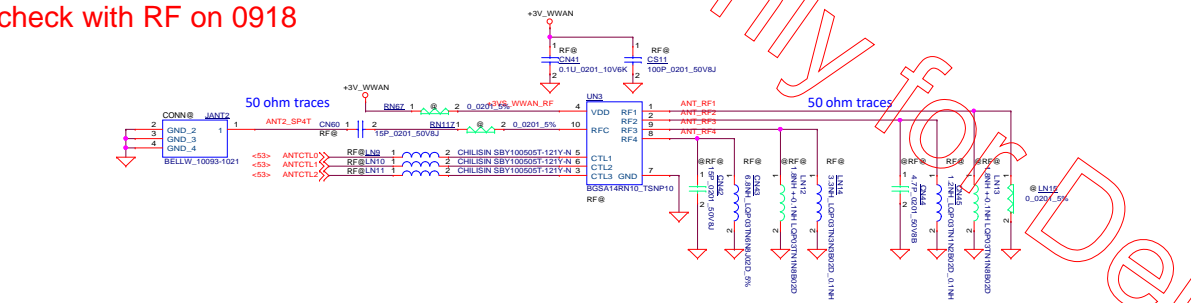
JLTE1/2 CONN



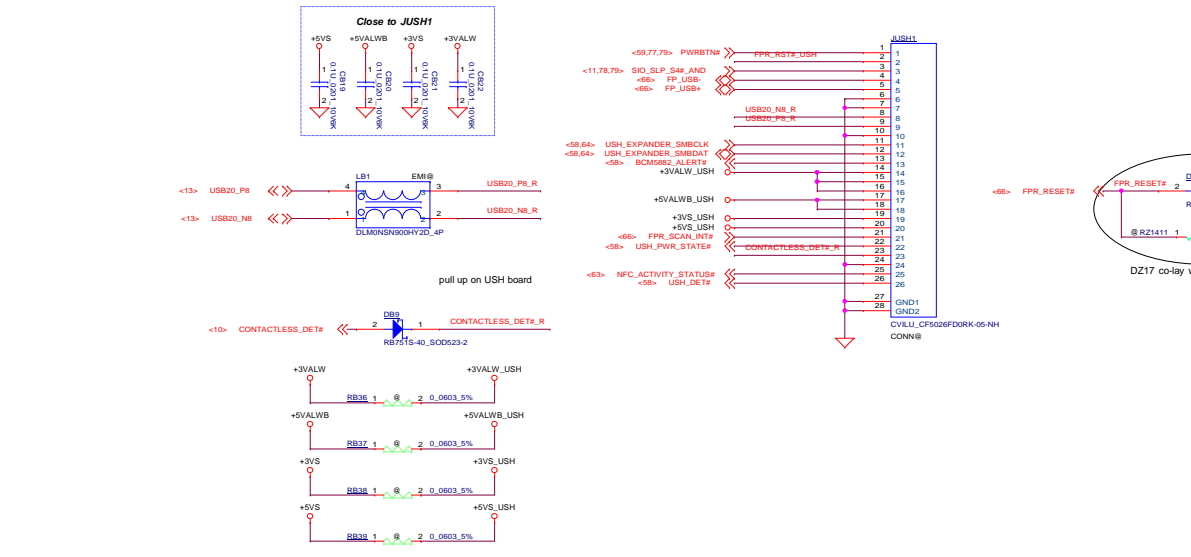
check with RF on 0213



LTE SW SP4T Tunnable IC  
check with RF on 0918



USH CONN



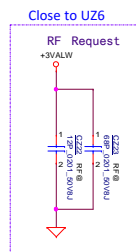
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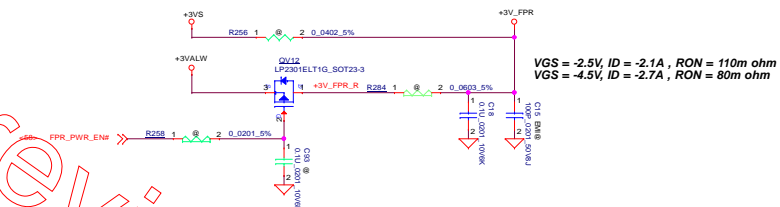
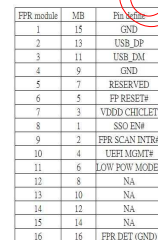
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		Wednesday, March 04, 2020		1.0(A00)	
				Sheet 65 of 100	

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[illegible]

***3V\_FPR***



FPR module	MB	Pin define
1	15	GND
2	13	USB_DP
3	11	USB_DM
4	9	GND
5	7	RESERVED
6	5	FP RESET#
7	3	VDD CHICLET
8	1	SSO EN#
9	2	FPR_SCAN_INTR#
10	4	UEFI_MGMT#
11	6	LOW_POWER_MODE
12	8	NA
13	10	NA
14	12	NA
15	14	NA
16	16	FPR_DET (GND)

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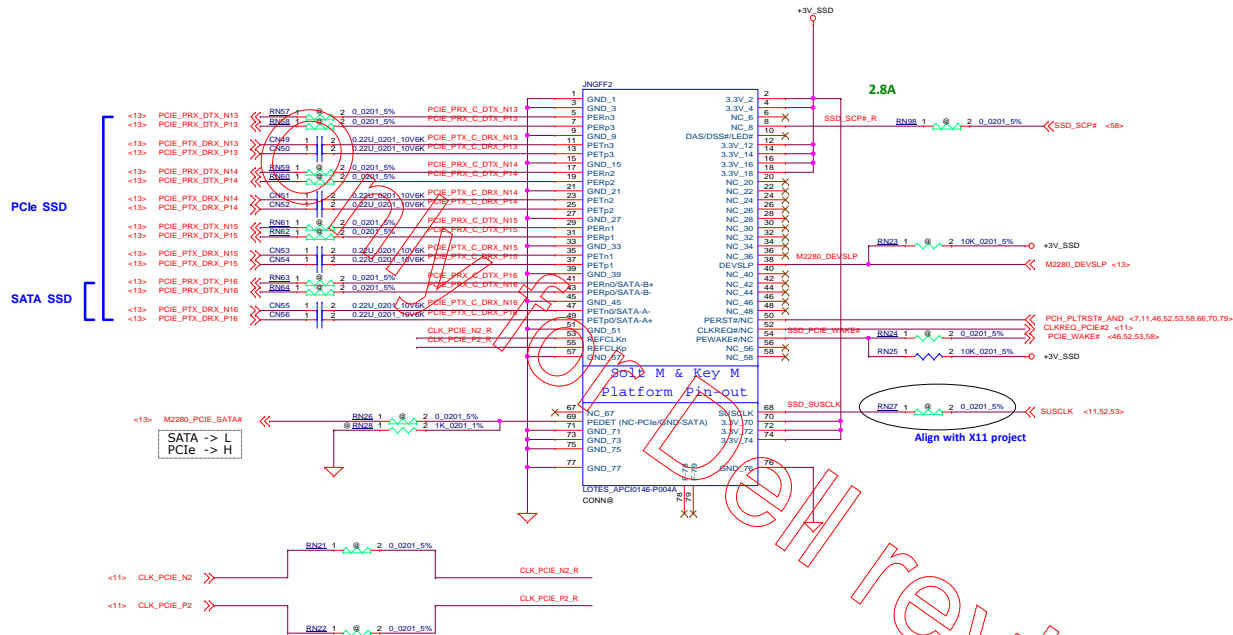
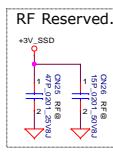
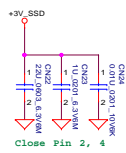
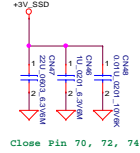
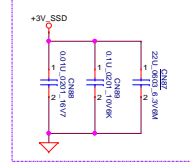
Title		
<b>P066 - TPM / Sensors / FPR</b>		
Size	Document Number	Rev
	<b>LA-J541P</b>	1.0(A)

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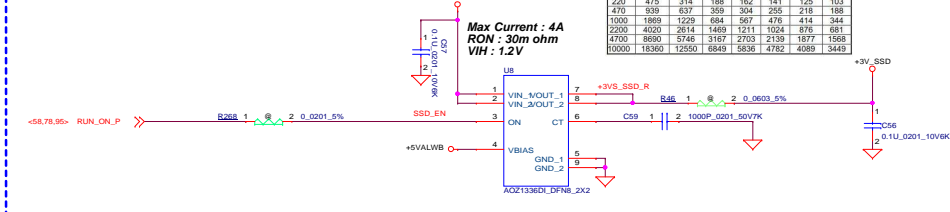
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# Add Power Decoupling for support Intel Teton Glacier

Place close JNGFF2 pin 12,14,16,18



3V\_SS



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				LA-J541P	
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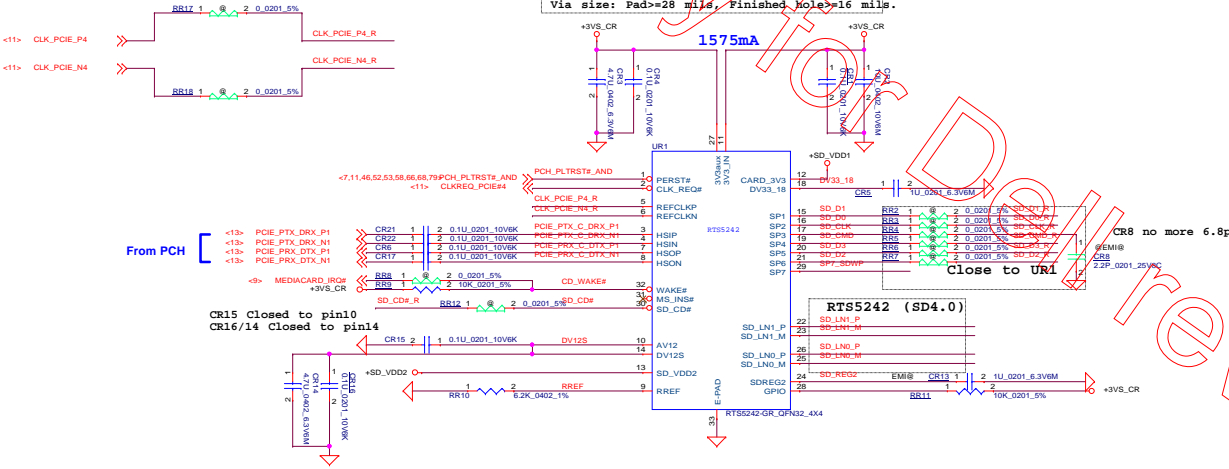
Check done by vendor on  
SN65 PCIe Redriver

Remove PCIe Redriver

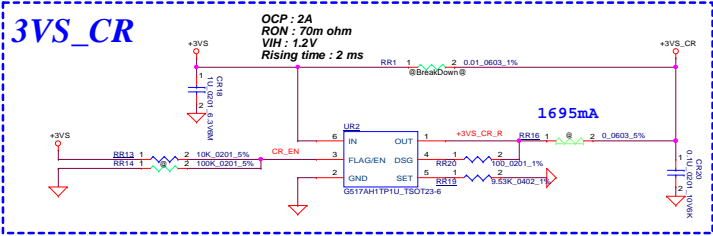
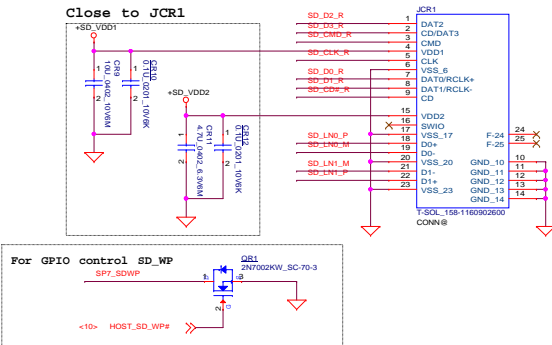
Check down by vendor on  
uSD Card Reader Controller/Connector

Controller

Pin11, pin12 trace fixed width is 40 mils.  
Pin27 trace fixed width is 30mils.  
Pin10, pin14, pin18 trace fixed width is 20 mils.  
Pin 9 trace fixed width is 12 mils.  
Trace routing length < 200mils.  
Via size: Pad=28 mils, Finished Hole=16 mils.

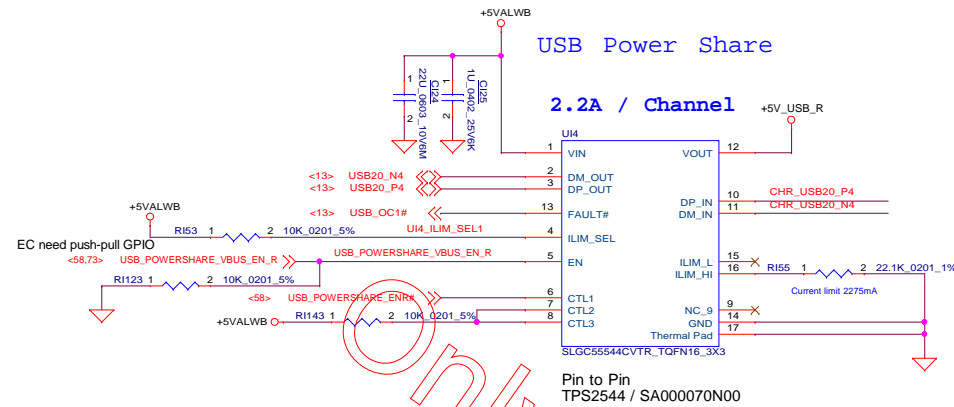


Connector

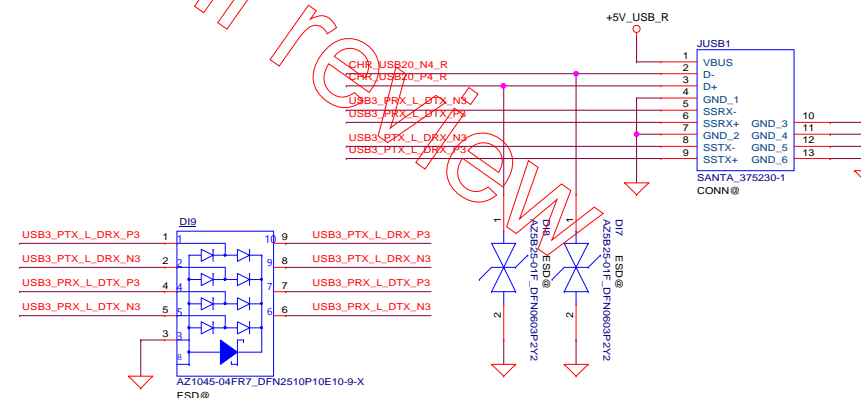
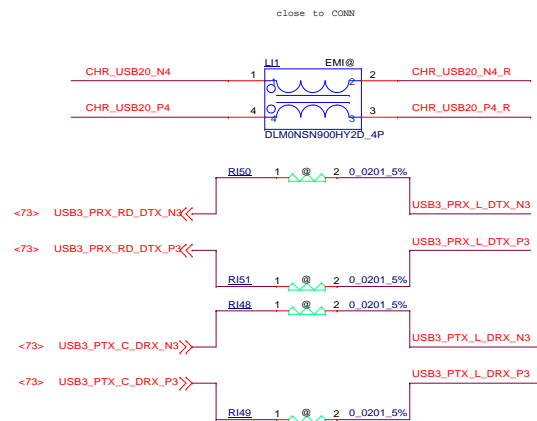
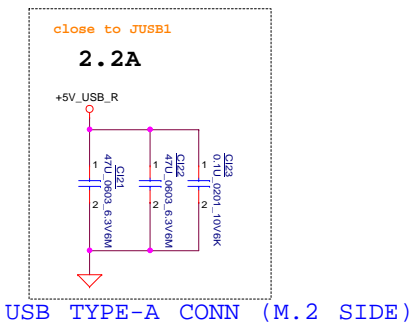


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				P070 - PCIe Retimer/ uSD RTSS24	
				Rev	
				1.00/000	
				Date: Wednesday, March 04, 2020	
				Sheet 70 of 100	

Check done by vendor on 0321  
USB Type-A Connector (M.2 SIDE



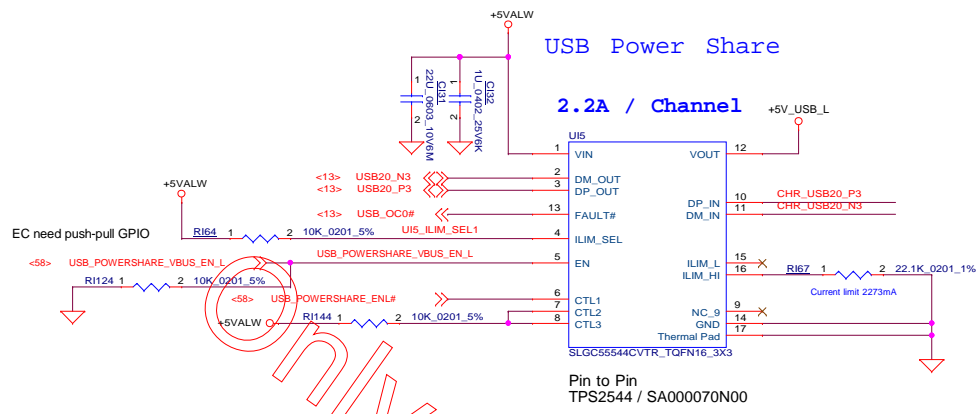
	CTL1	CTL2	CTL3	ILIM_SEL	MODE
	0	1	1	0	DCP_Auto
	0	1	1	1	DCP_Auto
	1	1	1	0	SDP
	1	1	1	1	CDP



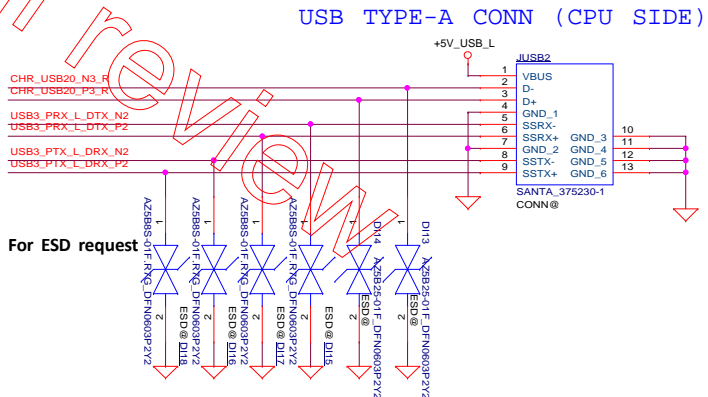
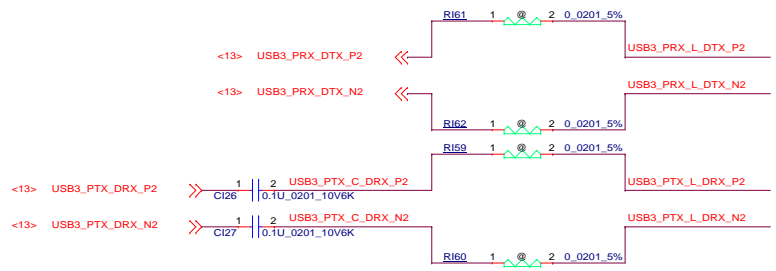
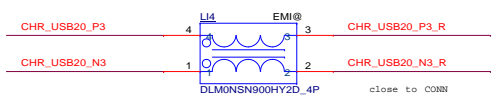
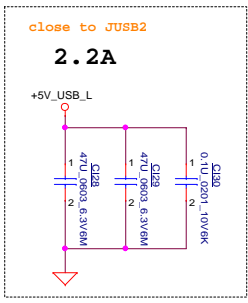
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# Check done by vendor on 0321

## USB Type-A Connector (CPU Side)



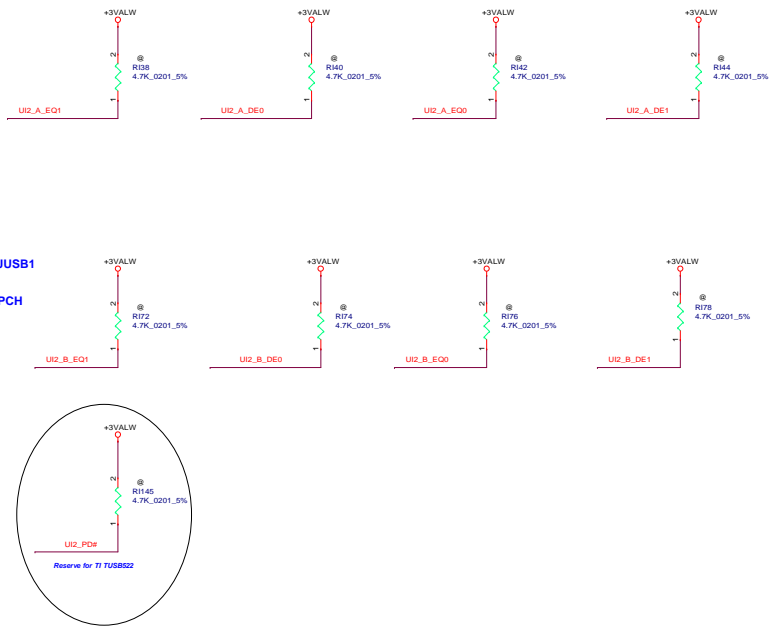
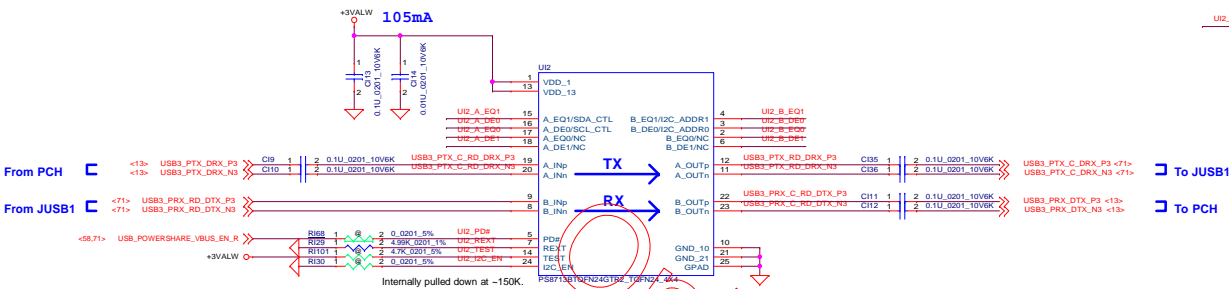
CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDP
1	1	1	1	CDP





Check done by vendor on 0309

USB3.0 Re-driver PS8713 (M.2 SIDE TO JUSB1)



Parade\_PS8713B

A_EQ1	A_EQ0	B_EQ1	B_EQ0	Recommended EQ	A_DE1	A_DE0	B_DE1	B_DE0	Recommended DE
0	0	0	0	loss up to 9.5dB	0	0	0	0	3.5dB de-emphasis
0	1	0	1	loss up to 13dB	0	1	0	1	No de-emphasis
1	0	1	0	loss up to 4.5dB	1	0	1	0	2.7dB de-emphasis
1	1	1	1	loss up to 7.5dB	1	1	1	1	5dB de-emphasis

Both A\_EQ&B\_EQ have internal pull-down 150k      Both A\_DE&B\_DE have internal pull-down 150k

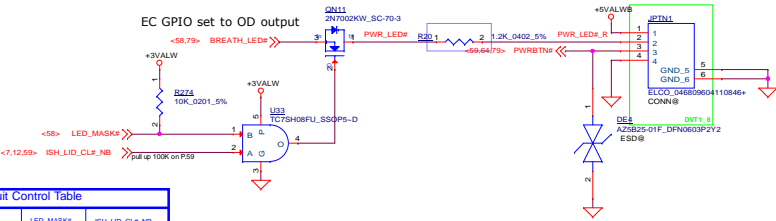
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				Rev	1.0(A00)



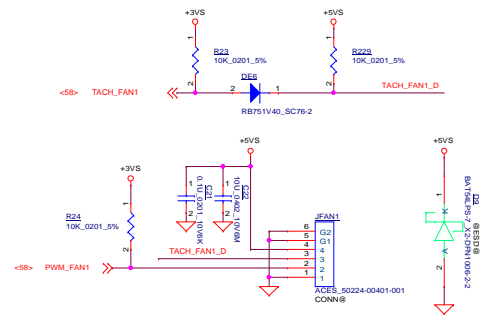


PW Switch Conn.



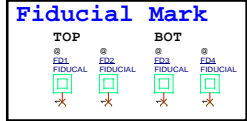
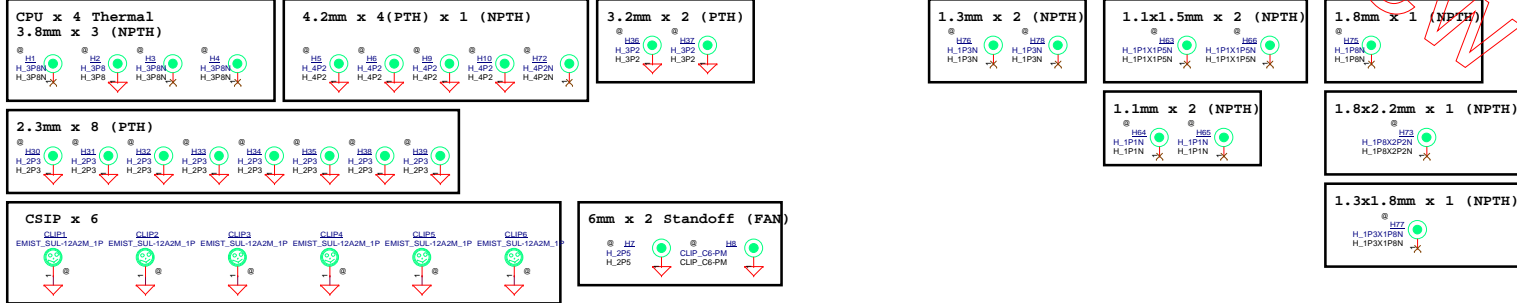
LED Circuit Control Table		
	LED_MASK	ISH_LID_CLF_NB
Mask All LEDs (Unidirectional)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Open)	1	1

FAN1 ??need to check pin define



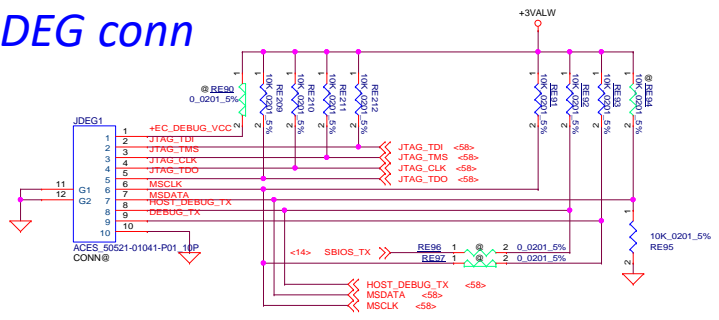
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Screw Hole For ME 0507-2 update

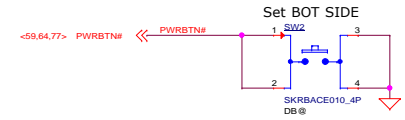




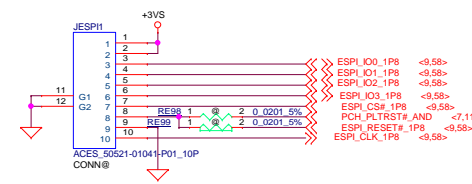
DEG conn



Test Power But t on

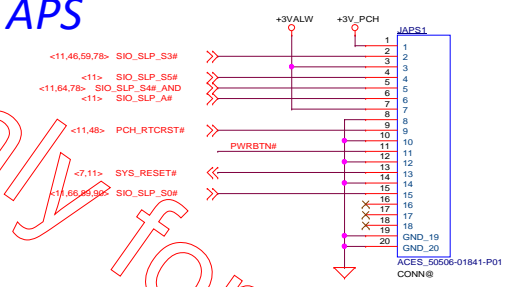


eSPI

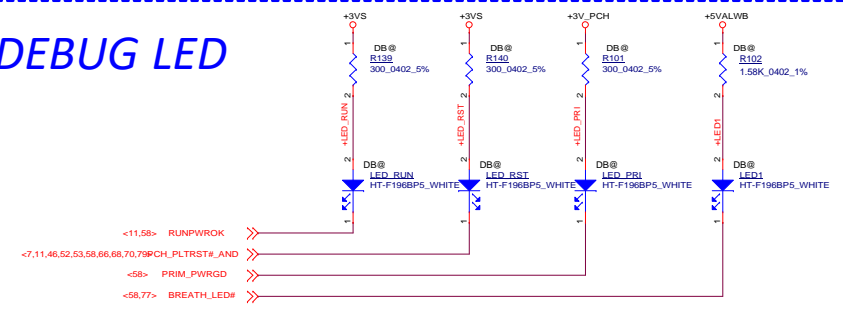


LPC_Support Debug	LPC	ESPI
1	+3VS	+3VS
2	+3VS	+3VS
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAMES	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLK	ESPI_CLK

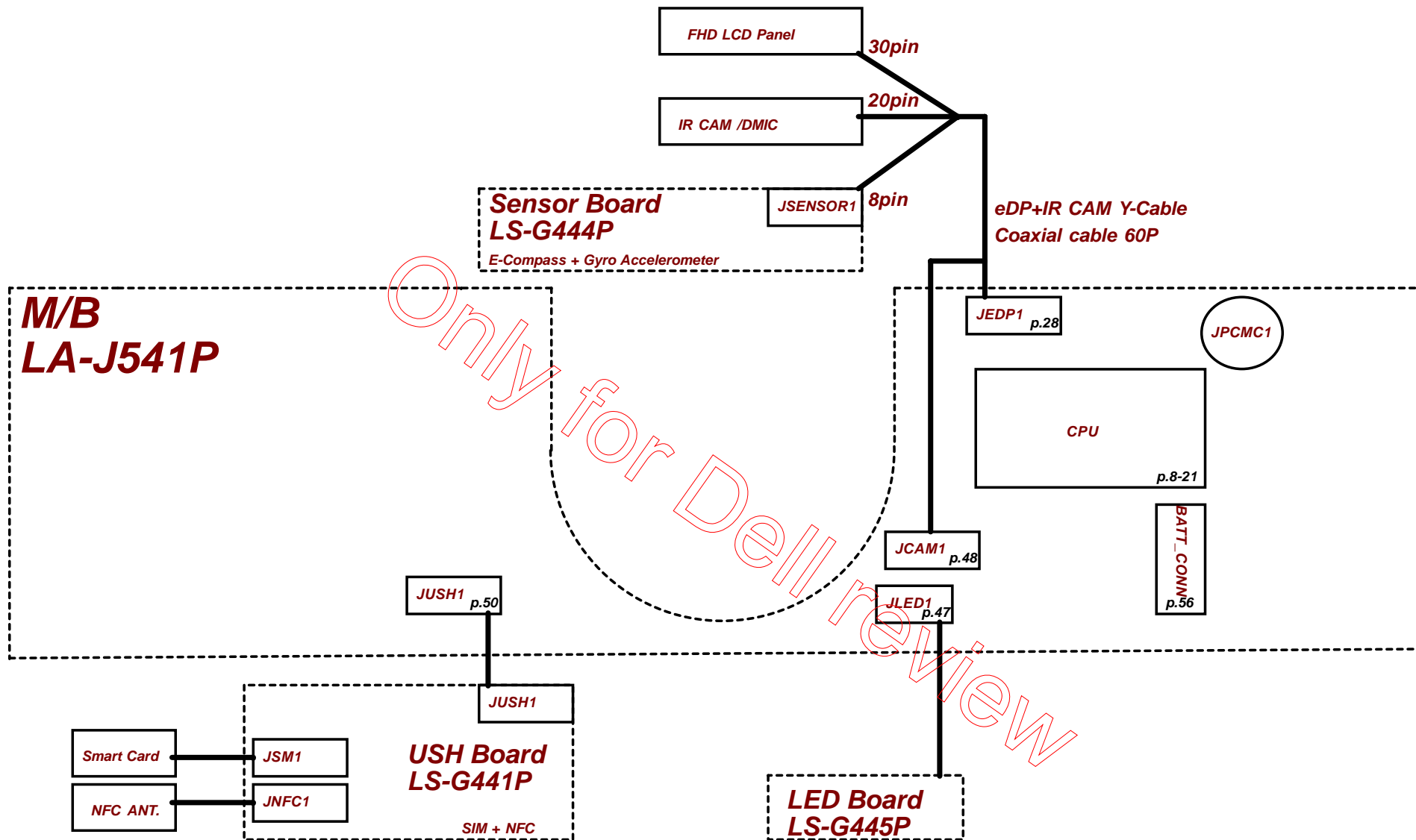
APS



DEBUG LED

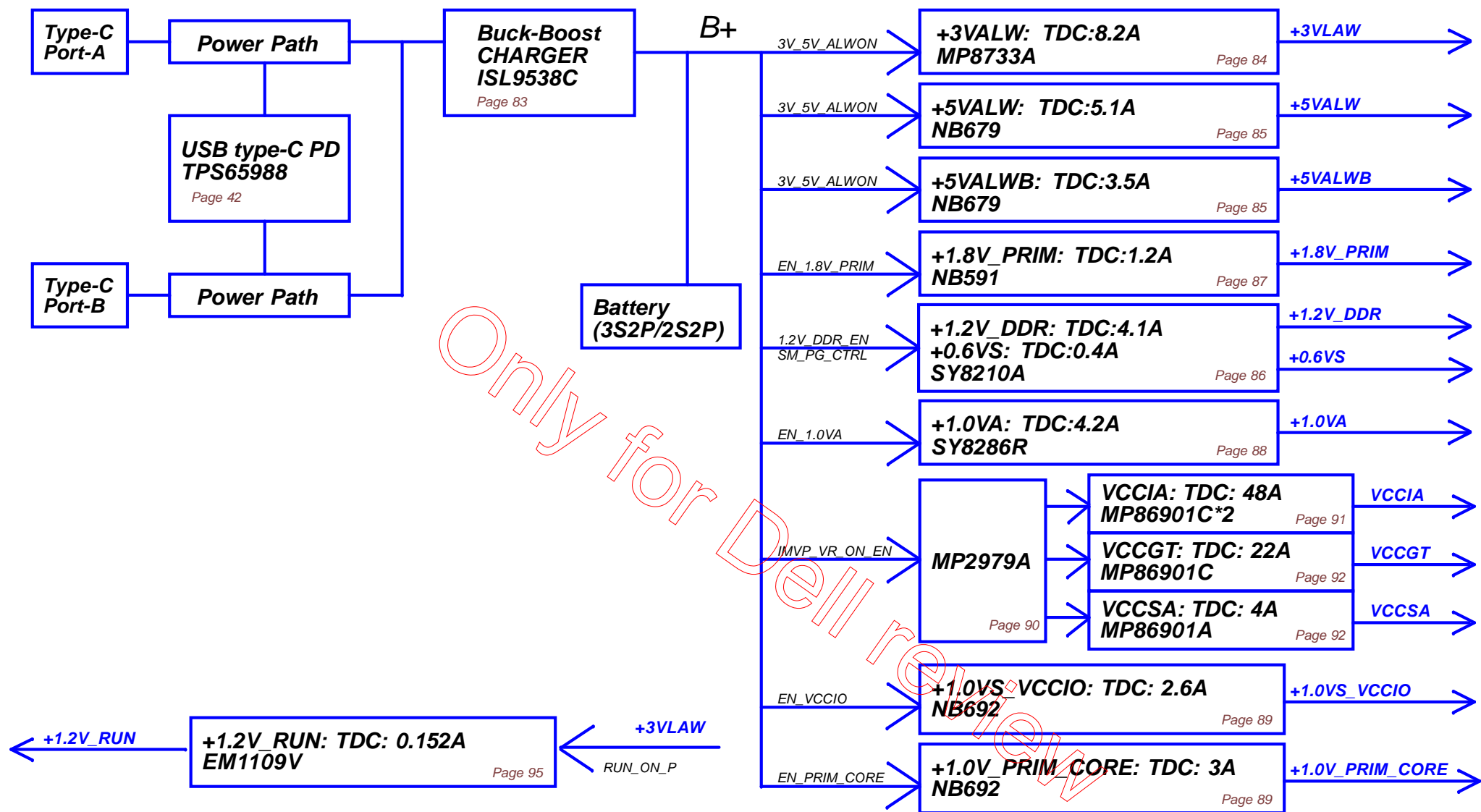


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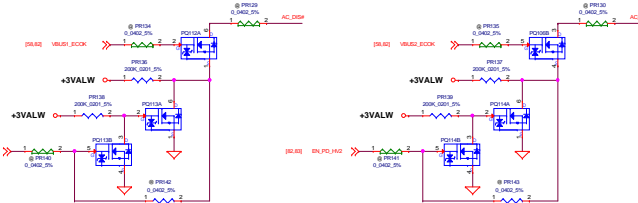
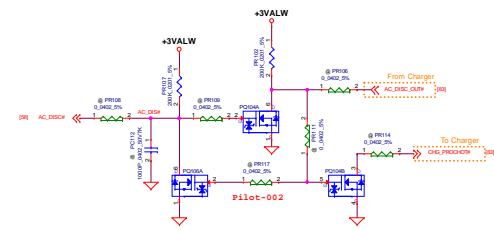
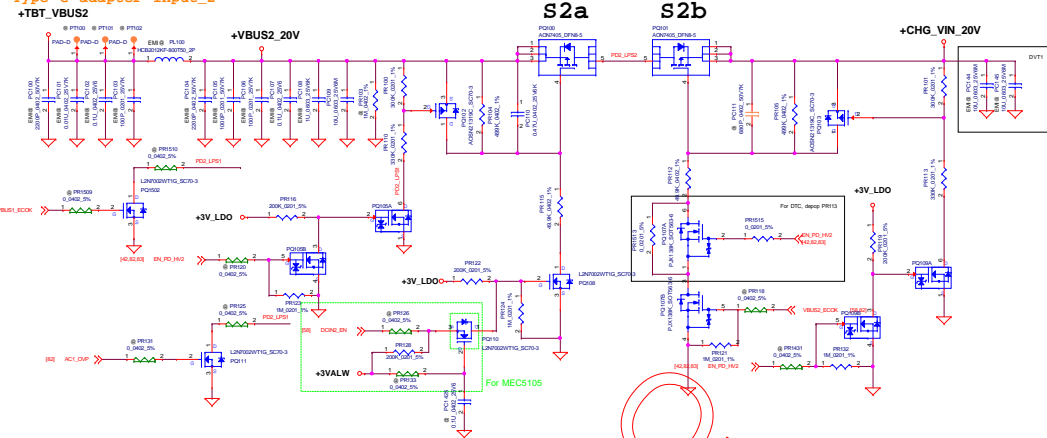
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										<b>P080 - DaughterB Block Diagram</b>	
										Size Document Number	
										<b>LA-J541P</b>	
										Date: Wednesday, March 04, 2020	
										Sheet 80 of 100	



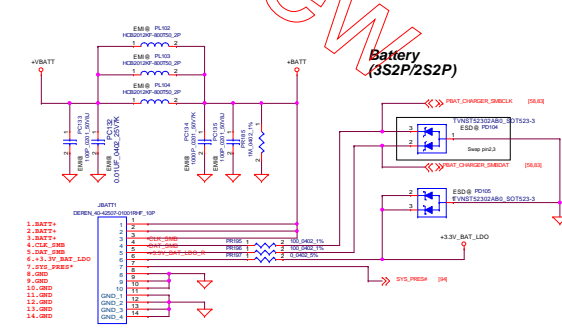
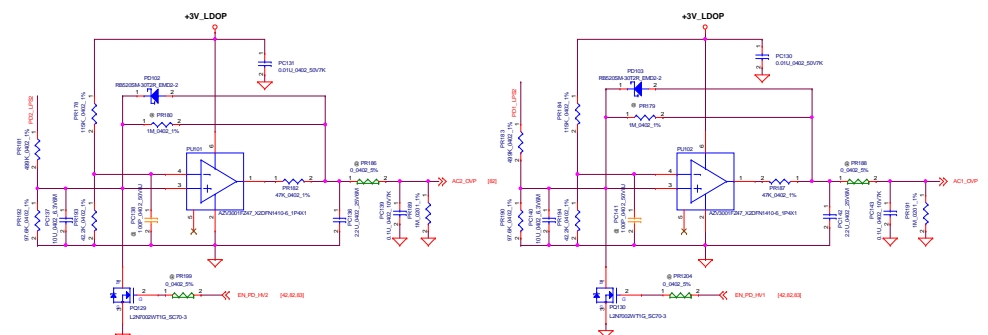
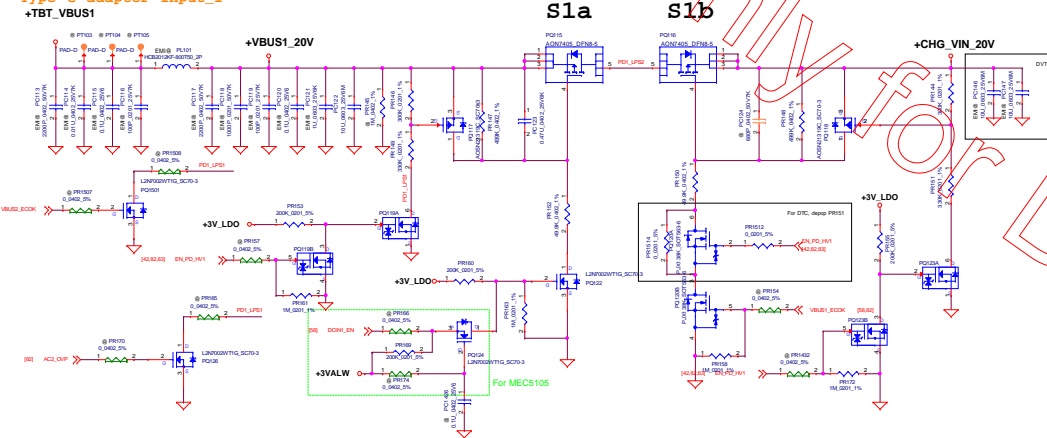


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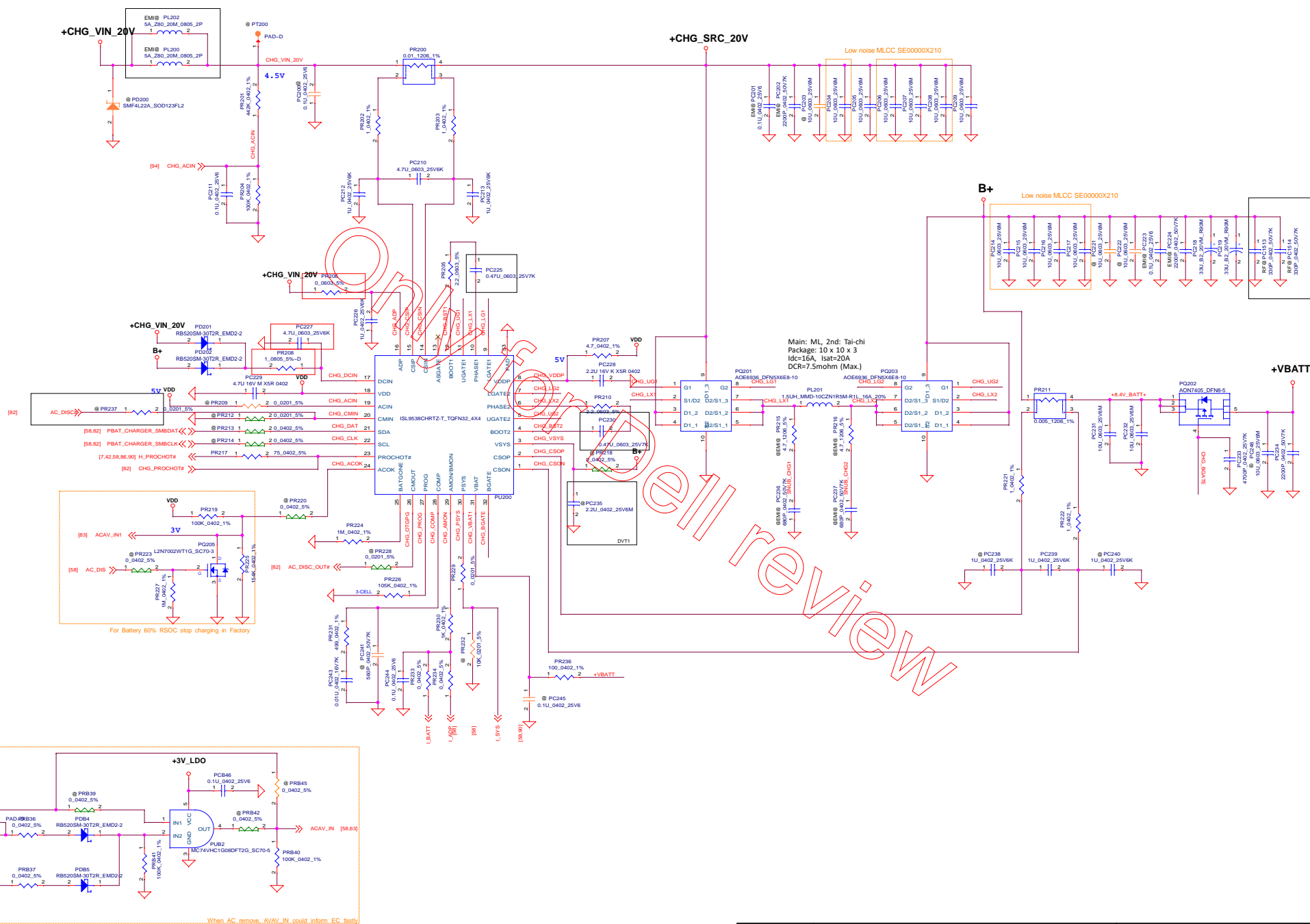
### Type C adapter input\_2



### Type C adapter input\_1



Charger controller(40.1), Support component(40.2)



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				Date: Wednesday, March 04, 2020		Sheet: 83 of 100

3V controller(35.1), Support component(35.2)

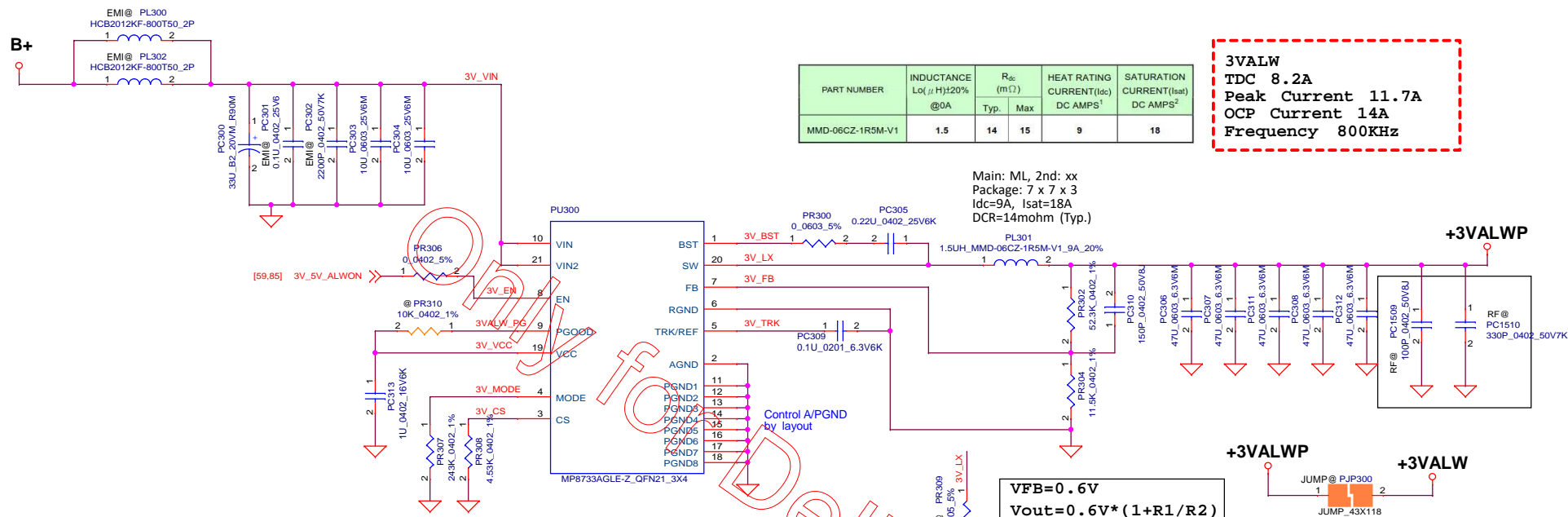


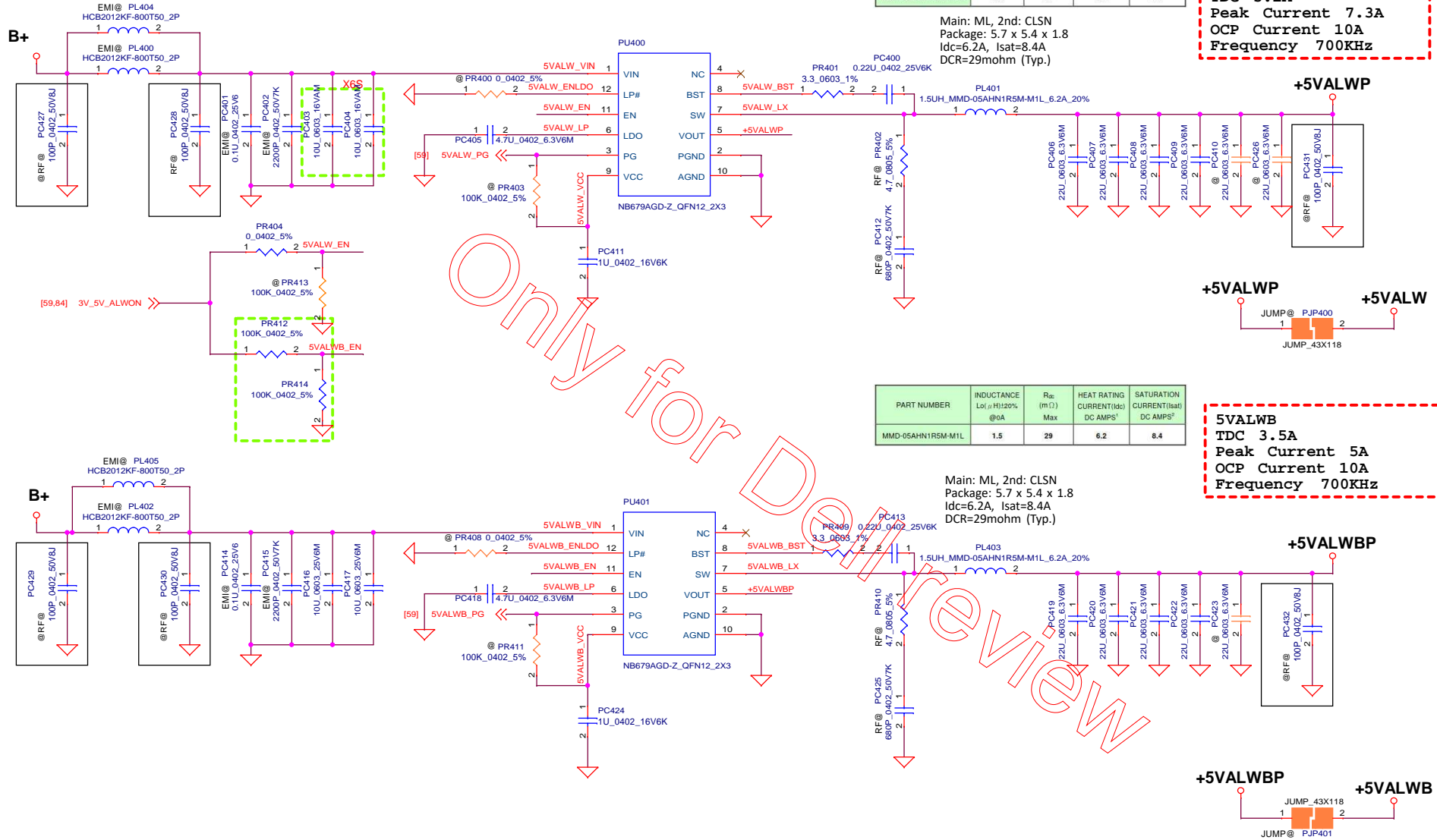
Table 1: MODE Selection

MODE	Light-Load Mode	Switching Frequency
VCC	Pulse skip	600 kHz
243k $\Omega$ ( $\pm 20\%$ ) to GND	Pulse skip	800 kHz
121k $\Omega$ ( $\pm 20\%$ ) to GND	Pulse skip	1000 kHz
GND	Forced CCM	600 kHz
30.1k $\Omega$ ( $\pm 20\%$ ) to GND	Forced CCM	800 kHz
60.4k $\Omega$ ( $\pm 20\%$ ) to GND	Forced CCM	1000 kHz

$$\begin{aligned} V_{FB} &= 0.6V \\ V_{out} &= 0.6V * (1 + R_1/R_2) \\ V_{out} &= 3.318V \end{aligned}$$

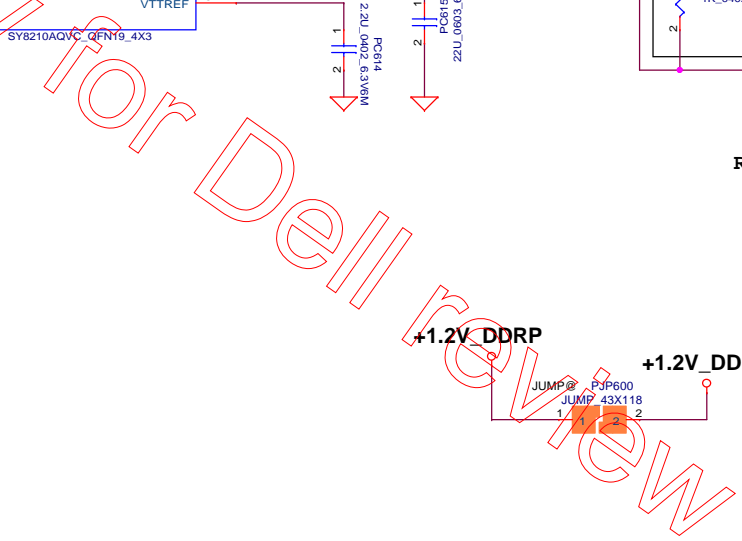
Diagram of a 2-to-1 multiplexer. The inputs are **+3VALWP** and **+3VALW**. The outputs are labeled **1** and **2**. The output **1** is associated with the label **JUMP @PJP300** and the output **2** is associated with the label **JUMP\_43X118**.

# 5V controller(35.1), Support component(35.2)



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Size		Document Number		Rev	
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Wednesday, March 04, 2020		Sheet		85 of 100	

DDR controller(35.3), Support component(35.4)



SH000014W00  
Main: MagLayers, 2nd: CYN  
Package: 5.2 x 5.4 x 1.8  
dc=8A, Isat=9A  
OCR=17mohm (Max.)

SH000014W00  
Main: MagLayers, 2nd: CYN  
Package: 5.2 x 5.4 x 1.8  
dc=8A, Isat=9A  
OCR=17mohm (Max.)

$$\begin{aligned} V_{FB} &= 0.6V \\ V_{out} &= 0.6V \cdot (1 + R_1/R_2) \\ V_{out} &= 1.2V \end{aligned}$$

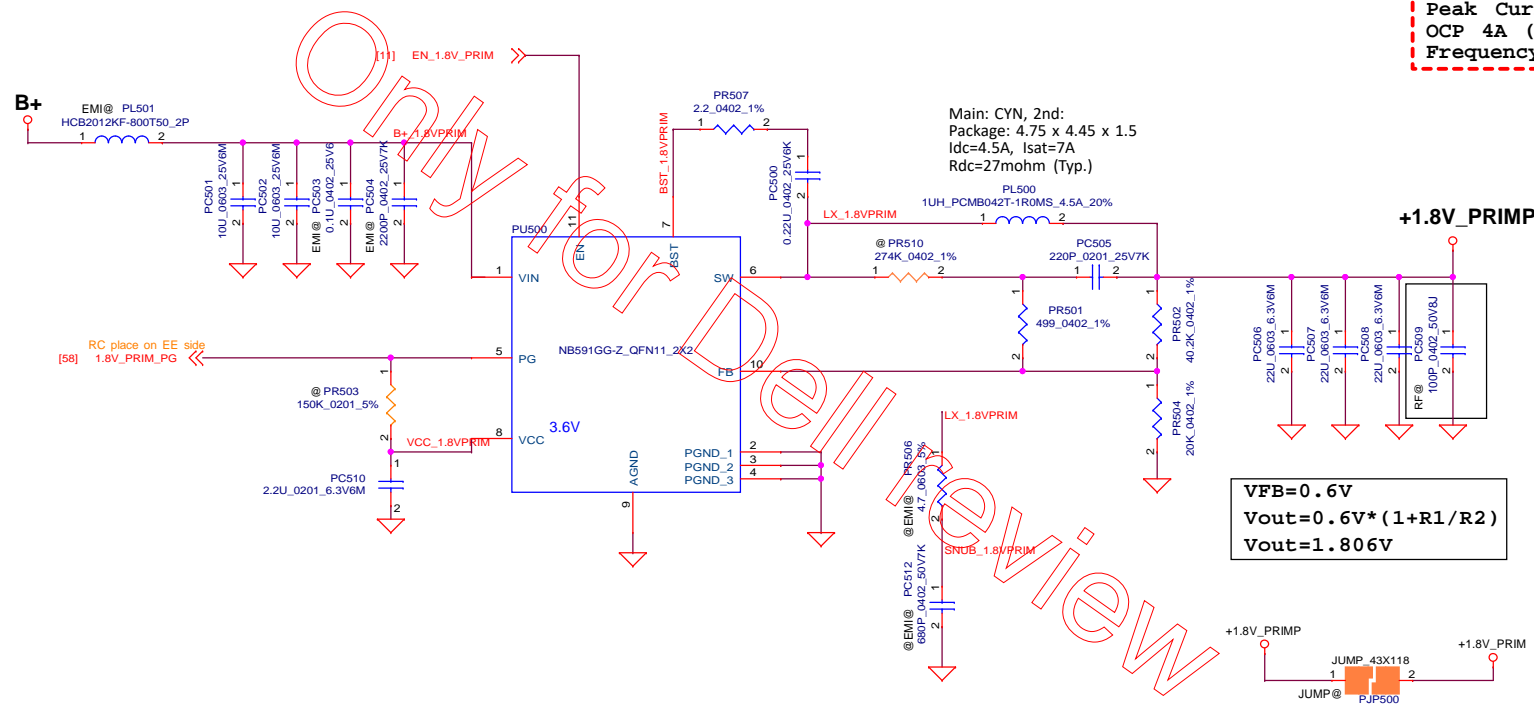
```
+1.2V_DDR
TDC 4.1A
Peak Current 5.8A
OCP Current 12A
Frequency 600KHz
```

+0.6VS  
TDC 0.4A  
Peak Current 0.6A  
OCP Current 2A (fix)  
Frequency 600KHz

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				Size	Document Number	Rev
				LA-J541P		1.0 (A00)
				Date:	Wednesday, March 04, 2020	Sheet 86 of 100

**+1.8V\_PRIM controller(35.13), Support component(35.14)**

```
1.8V_PRIM
TDC 1.2
Peak Current 1.6A
OCP 4A (Typ.)
Frequency 750KHz
```



$$\begin{aligned} V_{FB} &= 0.6V \\ V_{out} &= 0.6V * (1 + R_1/R_2) \\ V_{out} &= 1.806V \end{aligned}$$

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				Size	Document Number	Rev
				LA-J541P		1.0 (A00)
				Date:	Wednesday, March 04, 2020	Sheet 87 of 100

1.05V controller(35.5), Support component(35.6)

+1.0VA  
TDC 3.65A  
Peak Current 5.2A  
OCP current 9.0A  
Frequency 500KHz

EN :H>0.8V ; L<0.4V

EN pin don't floating  
If have pull down resistor at HW side,  
please delete PR604.

The current limit is set to 6A, 9A or 12A when this pin  
is pull low, floating or pull high.

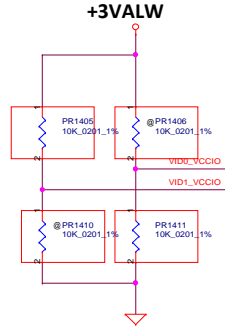
$$V_{out} = 0.6V * \left( \frac{1+R1/R2}{1+(15/20)} \right)$$

$$V_{out} = 1.05V$$

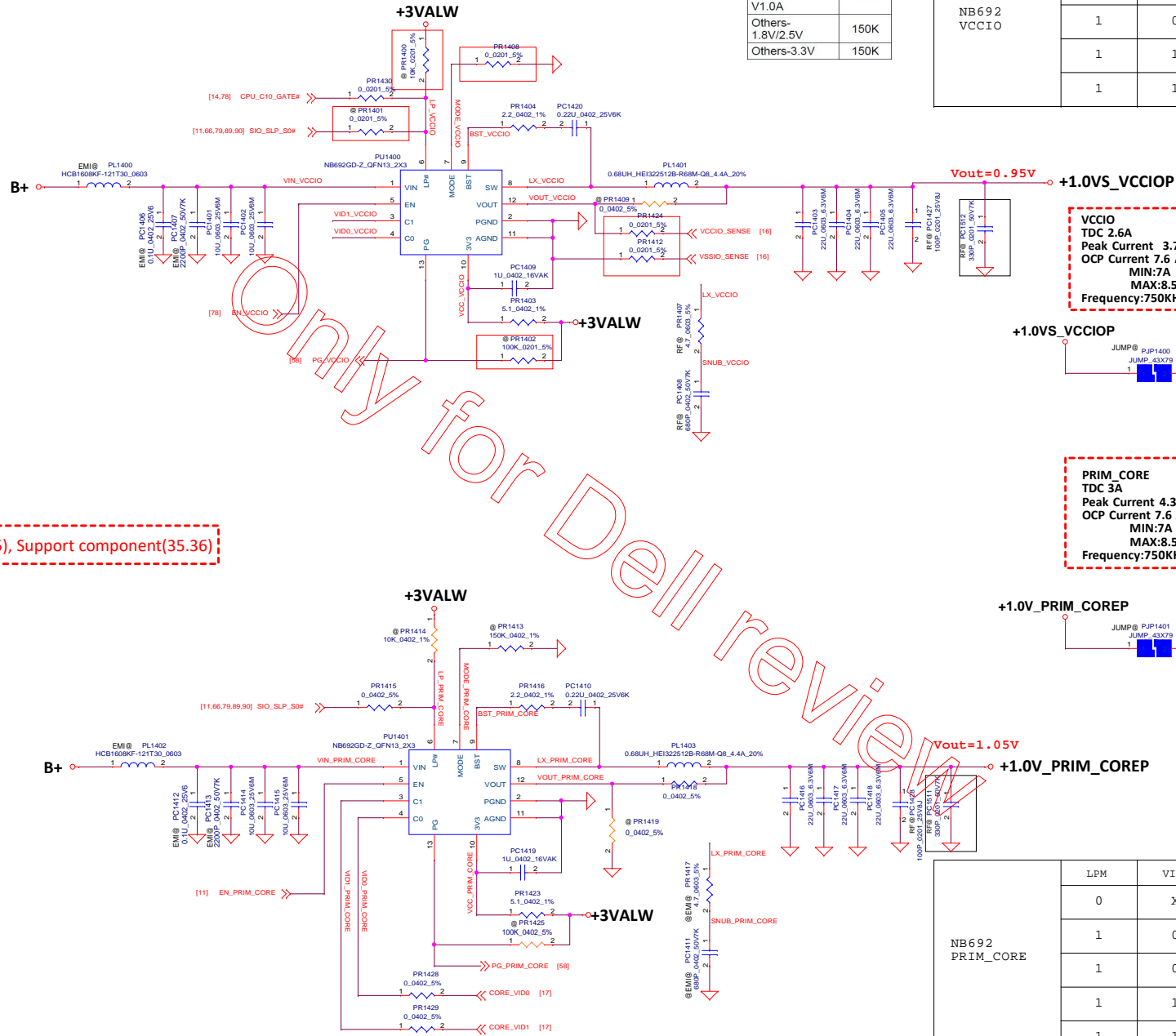
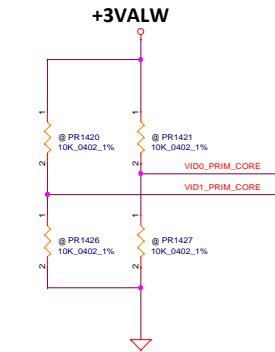
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	+IVALW (SY8286)
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				Rev	1.0 (A01)
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VCCIO controller(35.37), Support component(35.38)



+1.0V\_PROM controller(35.35), Support component(35.36)



V <sub>OUT</sub> (V)	R <sub>Mode</sub> (Ω)
VCCIO	0
PRIMCORE	Float
EDRAM/EOPIO/V1.0A	100K
Others-1.8V/2.5V	150K
Others-3.3V	150K

	LPM	VID1	VID0	V <sub>out</sub>
NB692 VCCIO	0	X	X	0 (LPM)
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

VCCIO  
TDC 2.6A  
Peak Current 3.7 A  
OCP Current 7.6 A Fix by IC  
MIN:7A  
MAX:8.5A  
Frequency:750KHz

PRIM\_CORE  
TDC 3A  
Peak Current 4.3 A  
OCP Current 7.6 A Fix by IC  
MIN:7A  
MAX:8.5A  
Frequency:750KHz

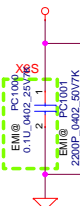
	LPM	VID1	VID0	V <sub>out</sub>
NB692 PRIM_CORE	0	X	X	0.75 (LPM)
	1	0	0	0.9
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05

+1.0VS\_VCCIO controller(35.21), Support component(35.22)  
+1.0V\_PRIM\_CORE controller(35.23), Support component(35.24)

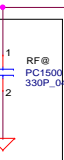


VCC\_CORE Dr. MOS (36.2), Support component(36.3)

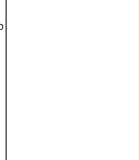
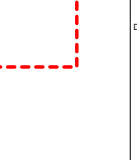
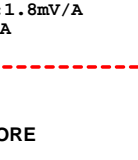
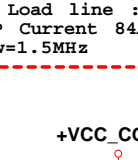
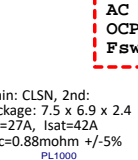
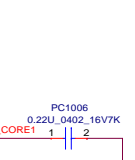
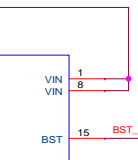
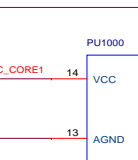
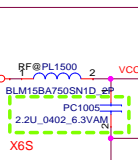
IA1\_B+



low noise(X6S)



+3VALW

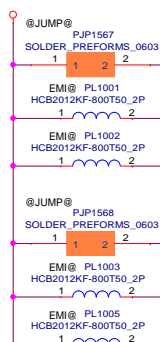


VCCIA (Base on PDG rev 0.9)  
Peak Current 70A (ICCmax)  
PL2 TDC :48A  
DC Load line :1.8mV/A  
AC Load line :1.8mV/A  
OCP Current 84A  
Fsw=1.5MHz

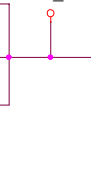
Main: CLSN, 2nd:  
Package: 7.5 x 6.9 x 2.4  
Idc=27A, Isat=42A  
Rdc=0.88mohm +/-5%

+VCC\_CORE

B+



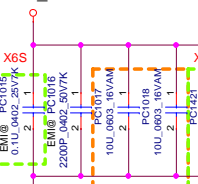
IA1\_B+



IA2\_B+

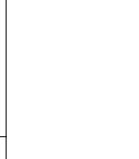
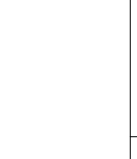
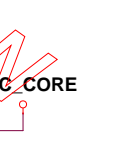
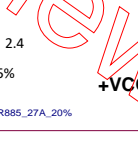
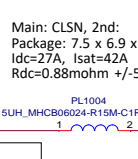
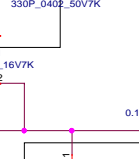
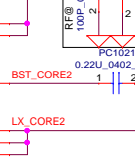
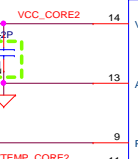


IA2\_B+



low noise(X6S)

+3VALW



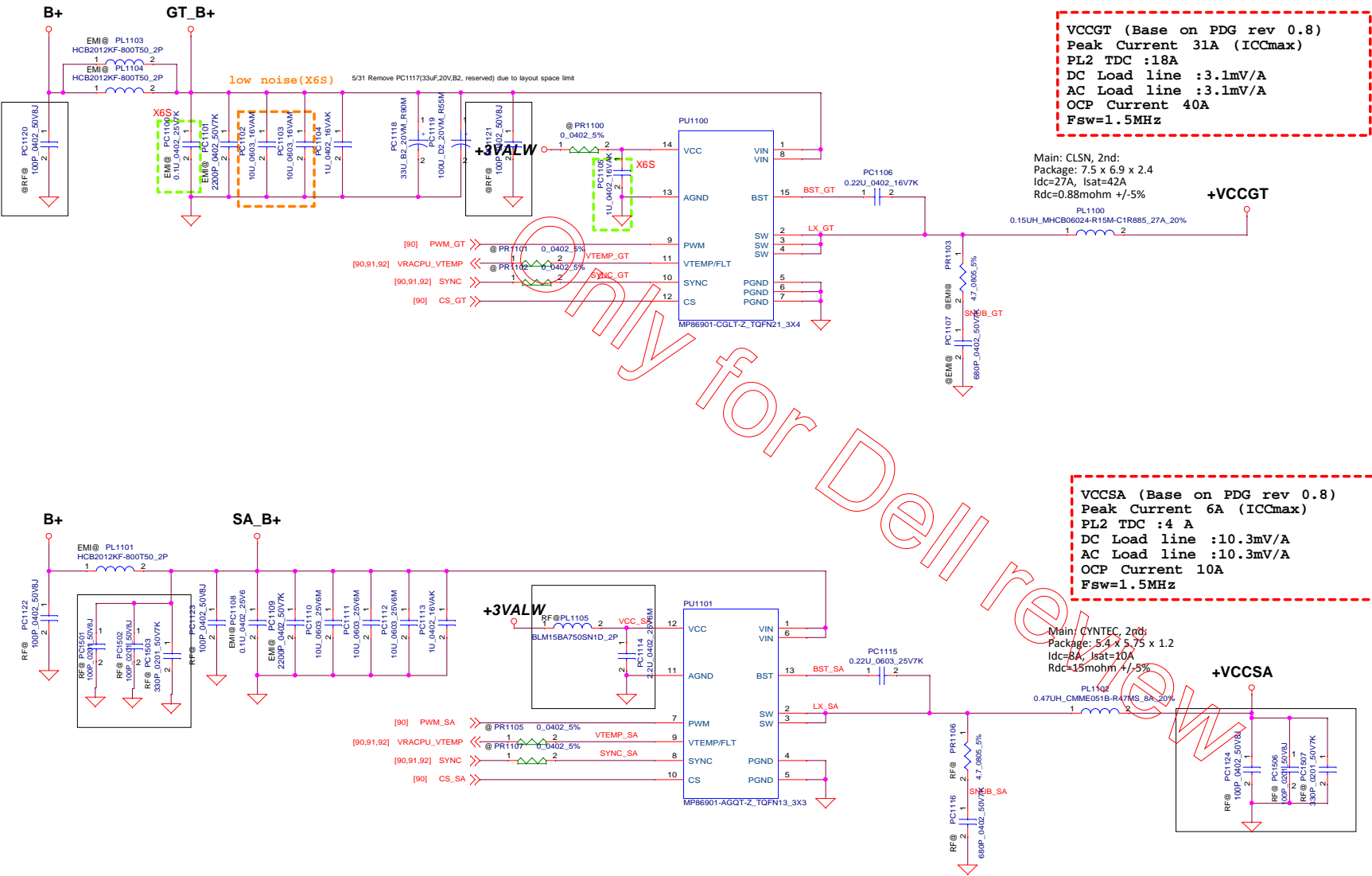
Main: CLSN, 2nd:  
Package: 7.5 x 6.9 x 2.4  
Idc=27A, Isat=42A  
Rdc=0.88mohm +/-5%

+VCC\_CORE

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				PWR_+VCORE		
				Size	Document Number	Rev
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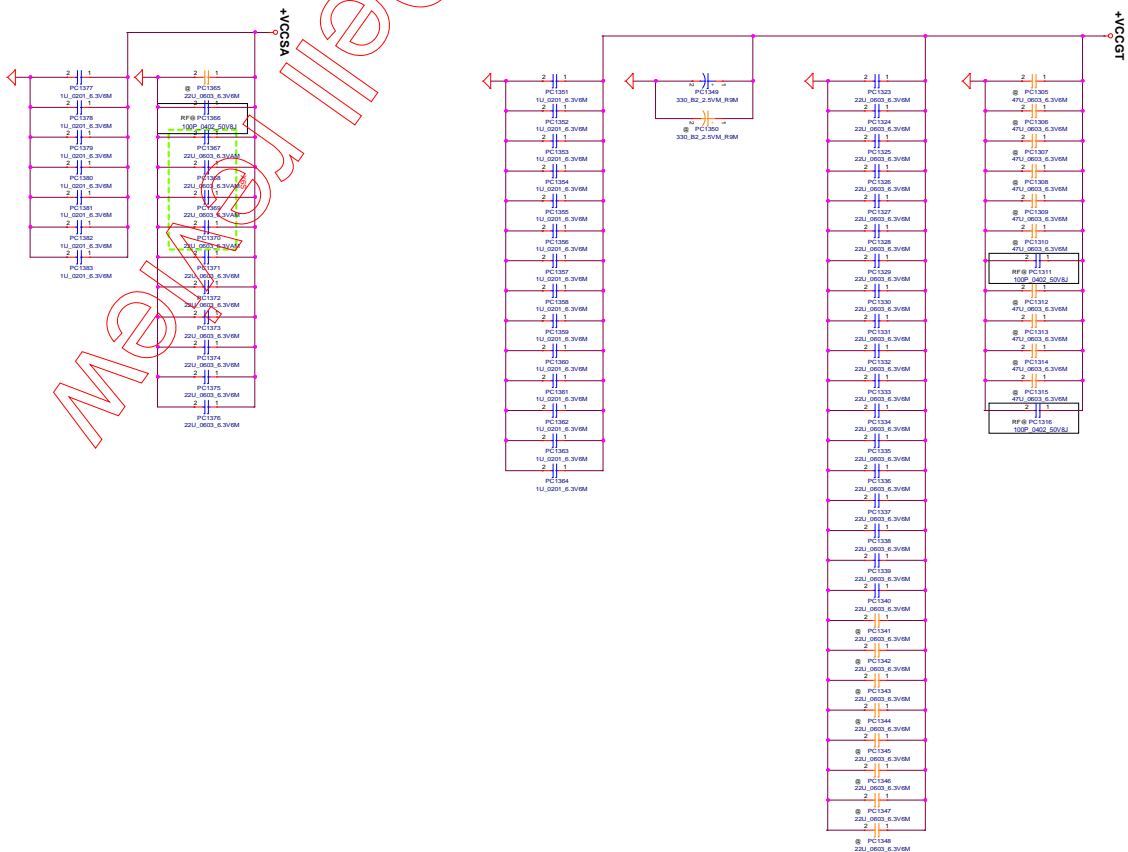
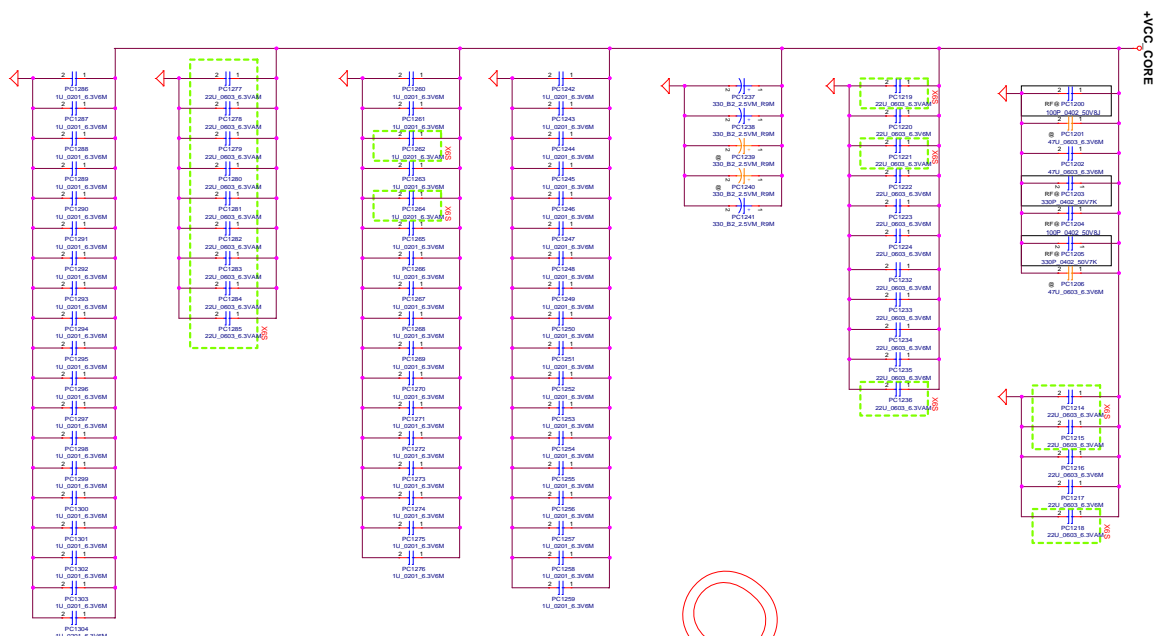
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VCC\_GT/SA Dr. MOS (36.2), Support component(36.3)



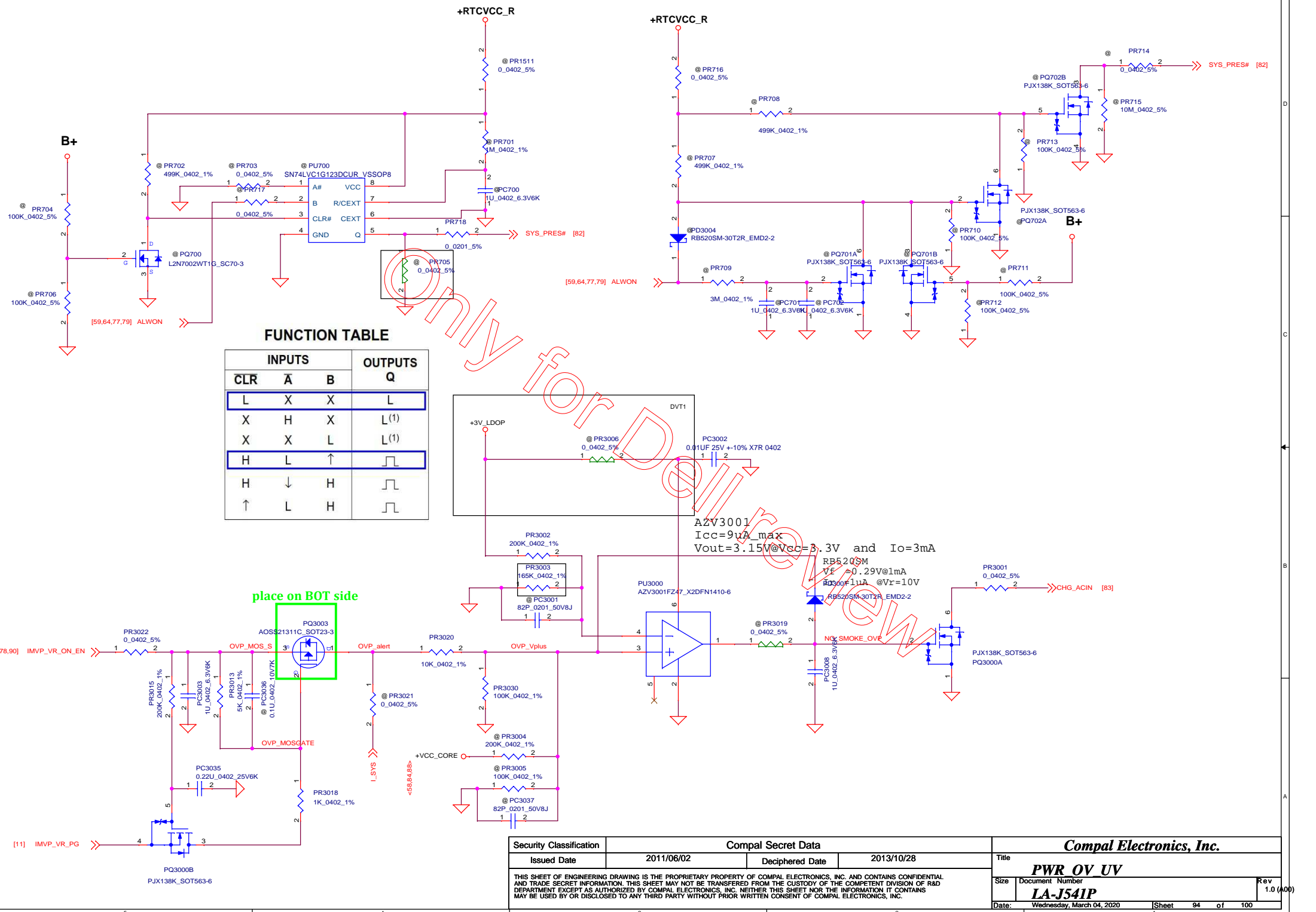
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VCC Core Output Cap(36.4), VCCGT Output Cap(36.5), VCCSA Output Cap(36.6)



VCC CORE output cap(36.4), VCC GT output cap(36.5), VCC SA output cap(36.6)

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Rev.	1.0	Rev.	1.0	Rev.	1.0
Rev.	1.0	Rev.	1.0	Rev.	1.0





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				Size	Document Number
				LA-J541P	
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				LA-J541P	
				Date:	Wednesday, March 04, 2020
				Sheet	98 of 100
				Rev	1.0 (A00)

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				Size	Document Number
				LA-J541P	
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# Version Change List

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P94	PWR	2019/09/24	Compal	VCORE OVP triggered when DC mode pwoer on	Change VCC power source from +3V_LDO to +3V_LDOP Add PR3006 0ohm. Change PR3003 from 120K to 165K	X01
2	P91	PWR	2019/09/24	Compal	For PD simulation	PR1567 change to PJP1567, PR1568 change to PJP1568	X01
3	P82	PWR	2019/09/24	Compal	Power path roll back to Gen10 design.	POP PR113, PR1513.PR151, PR1514	X01
4	P83	PWR	2019/09/24	Compal	Charger RC fine tune by vendor's request	PC227 change from 2.2uF to 4.7uF PC235 change from 0.01uF unpop to 2.2uF unpop	X01
5	P83	PWR	2019/09/24	Compal	For test purpose	Add PR237 unpop and connected to AC_DISC#	X01
6	P86	PWR	2019/10/2	Compal	For better efficiency	Change PL601 from 5x5x1.5 to 5x5x1.8 package	X01
7	P82	PWR	2019/10/2	Compal	For EMI request	Add PC144,PC145,PC146,PC147	X01
8	P83	PWR	2019/10/04	Compal	For thermal improve	Change Charger Choke PL201 from 10x10x2.4 to 10x10x3	X01
9	P87, P89, P92	PWR	2019/10/09	Compal	For RF request	Add PC1124, PC1427, PC1428, PC509 change from 22u 0603 (unpop) to 100P 0402 (pop)	X01
10	P94	PWR	2019/10/14	Compal	Advanced storage mode circuit fine tune	Add PR718, PR709 change to 3M ohm, PR715 change to 10M. PR701 change to 1M. PC700 change to 1uF. PR702 change to 499K	X01
11	P92, P93, P94	PWR	2019/10/14	Compal	For RF request	pop PR1012/PC1022,PR402/PC412,PR410/PC425,PR309/PC314, PR1003/PC1007,PR1106/PC1116,PR1407/PC1408. Change PC1311,PC1316 to 100P_0402. pop PC1204/PC1123,PC428, PC1423,PC1122,PC1424. Change PR1104 to PL1105 Bead, PC1114 change to 2.2uF.	X01
12	P90	PWR	2019/10/14	Compal	DC load line of VCCSA fine tune	PR943 change from 8.2K to 7.87K ohm.	X01
13	P94	PWR	2019/11/28	Compal	Battery roll back to standard storage mode.Remove one-shot IC circuits.	PR705 change to 0ohm, de-pop PU700 PR704 PR1511 PR716 PR707 PR708 PR709 PD3004 PC701 PQ701 PQ702 PR711 PR712 PR714 PR715	X03
14	P91, 92	PWR	2019/11/28	Compal	Material shortage	Change PC1006 PC1021 PC1106 from 0.22u 25V to 0.22u 16V	X03
15	P82, 94	PWR	2019/11/28	Compal	To meet MOSFET ESD(HBM) spec	Change PQ3003 from SB934090000 to SB00001SS00, PQ102 PQ103 PQ117 PQ118 from SB000006000 to SB00001SU00	X03
16	All	PWR	2019/12/3	Compal	RF request	1.Pop PC1023,PC1024,PC1026 2.Add PC1500,PC1501.PC1502,PC1503,PC1504,PC1505,PC1506, PC1507,PC1508,PC1509,PC1510,PC1511,PC1512,PC1513,PC1514. 3.PR1000 change to PL1500(BLM15BA750SN1), PR1009 change to PL1501(BLM15BA750SN1). (PC1005,PC1020 change from 1uF to 2.2uF). 4.PC1200,PC1366 change to 100PF 0402 package. 5.PC1203,PC1205 change to 330P 0402 package.	X03
17	All	PWR	2020/1/13	Compal	De-pop PR701,PR702,PR703,PR706 PR717,PC700,PQ700. PR705 change to 0ohm_short_pad	<div>Security Classification</div> <div>Issued Date</div> <div>Deciphered Date</div> <div>2022/12/31</div> <div>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</div> <div>Compal Secret Data</div> <div>Compal Electronics, Inc.</div> <div>P100 PWR PIR</div> <div>LA-J541P</div> <div>Rev 1.0 (A00)</div> <div>Date: Wednesday, March 04, 2020</div> <div>Sheet 100 of 100</div>	

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